

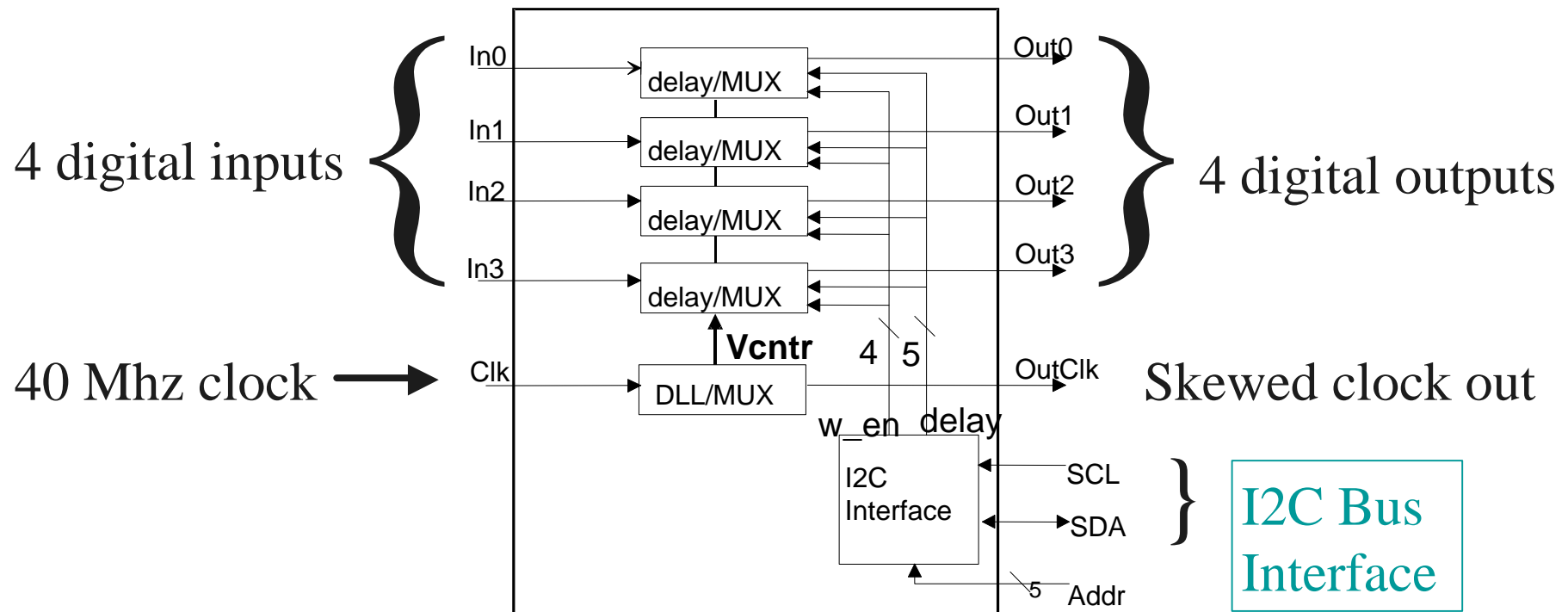
4 Channel Programmable Delay Generation ASIC

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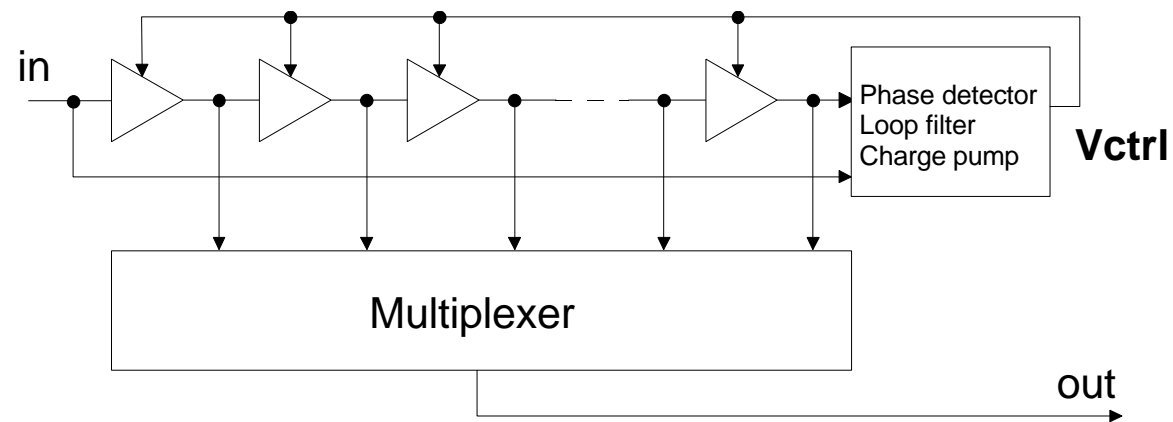
Delaychip Overview

- ✓ Delays Digital signals
- ✓ Delay can be programmed in 1ns steps
- ✓ 4+1 independent delay channels
- ✓ Needs 40Mhz clock as timing reference
- ✓ Programmed via I2C interface
- ✓ 4 bit I2C address space

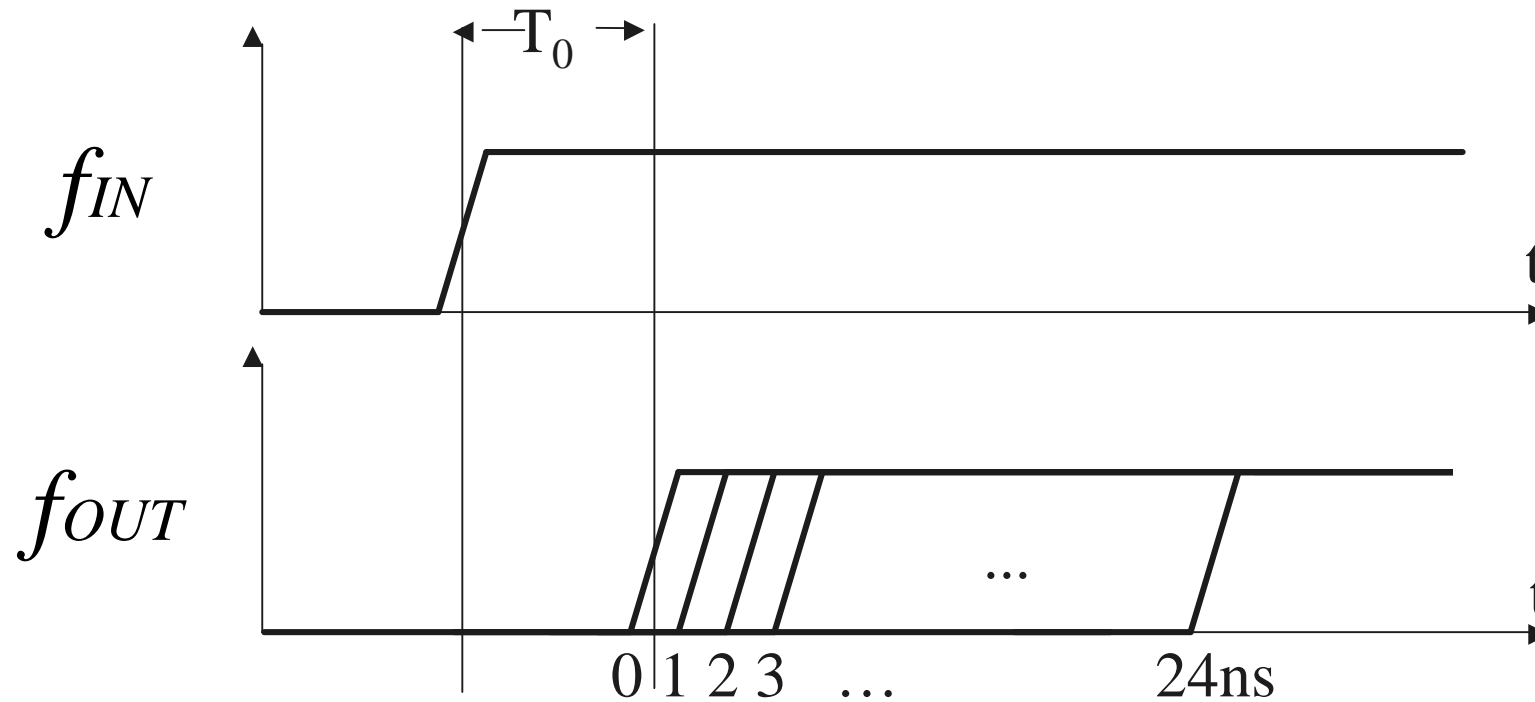
Delaychip Block diagram



Delay Locked Loop (DLL)



Timing diagram



I²C Command word format

Data Format:



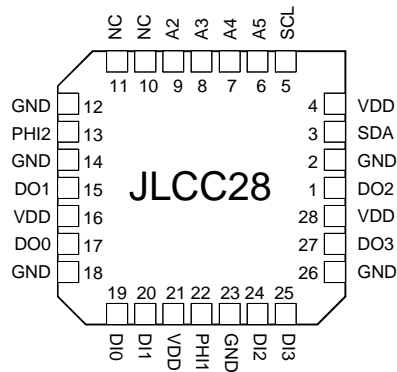
←
Bit 7-5 : device select

000	signal	1
001	“	2
010	“	3
011	“	4
100	“	CLK

→
Bit 4-0: delay select

0-24	: delay (0-24ns)
25 : 0	(disable output)
27 : 1	

Specifications



Supply voltage:

3.3±0.2 V

Input Clock frequency

40 MHz

Signaling

Low V CMOS

Chip size:

2.6x2.3 mm²

Package:

28 pin J-leaded
ceramic

Current consumption

DLL only:

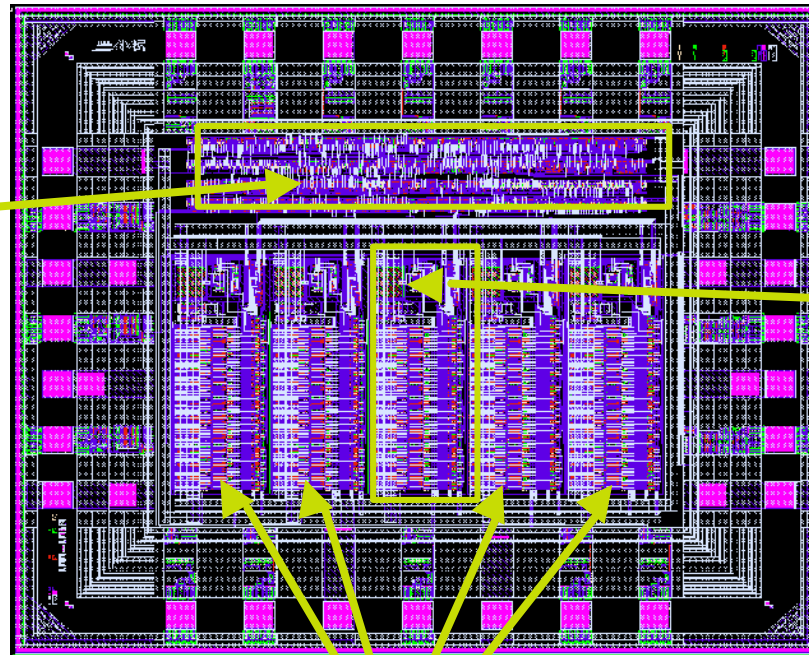
3mA

1 Delay channel:

3mA+75μA/Mhz

Delaychip Layout

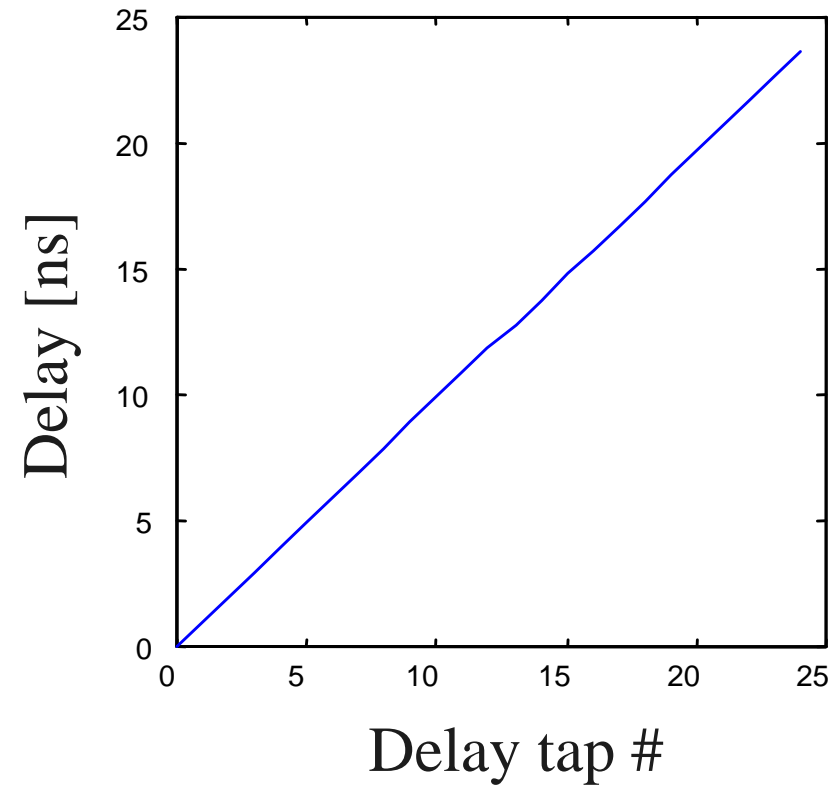
I2C and
initialisation
logic



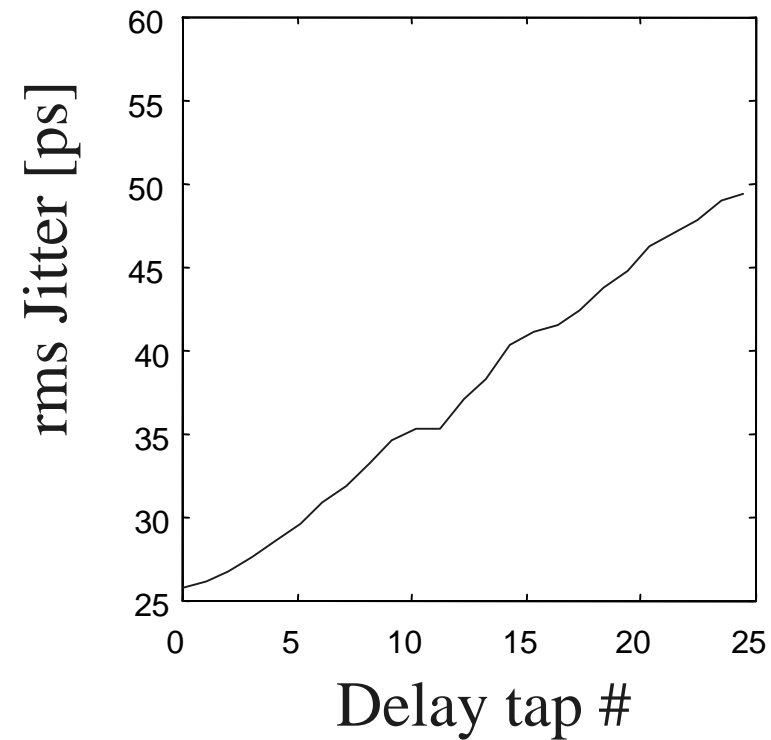
Delay-locked
Loop

Matched delay lines

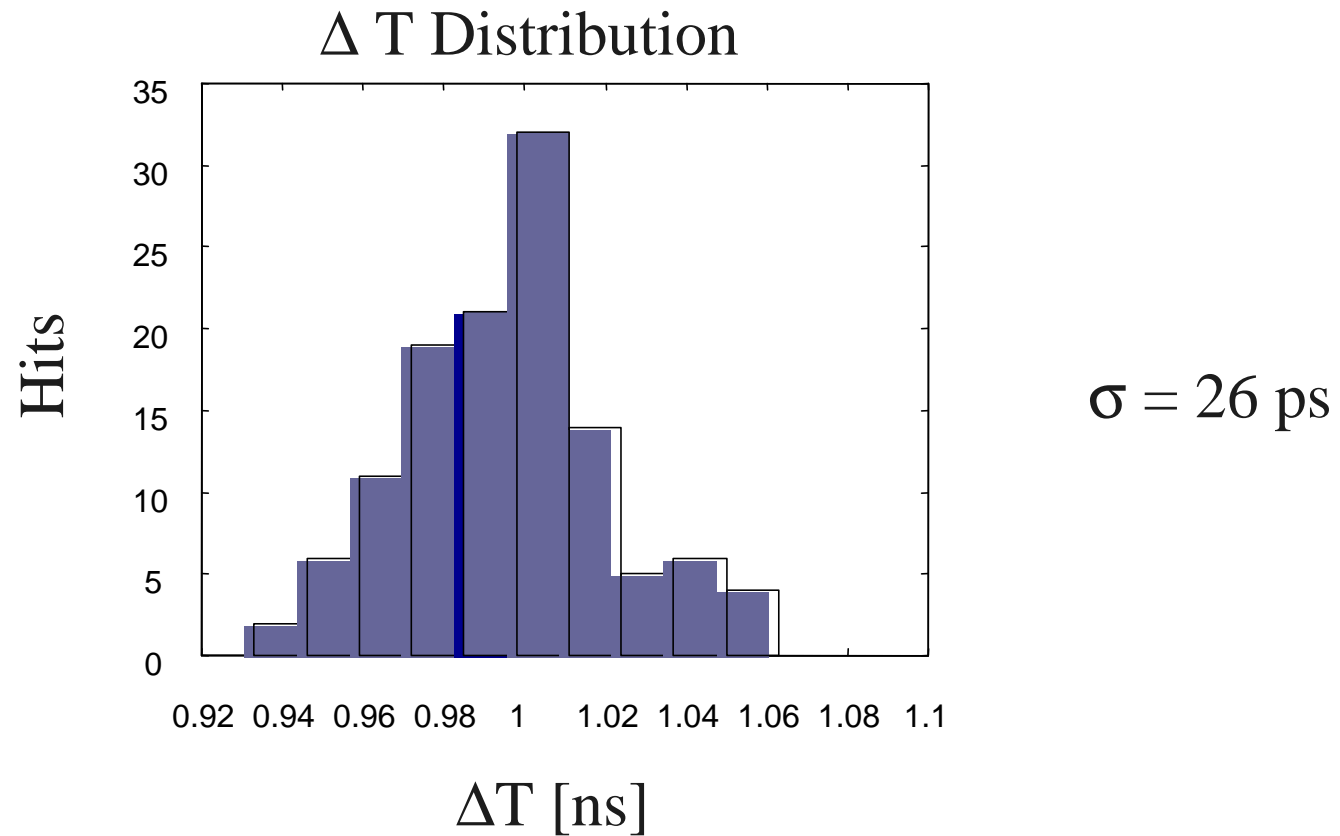
Measured Delay vs. programmed delay



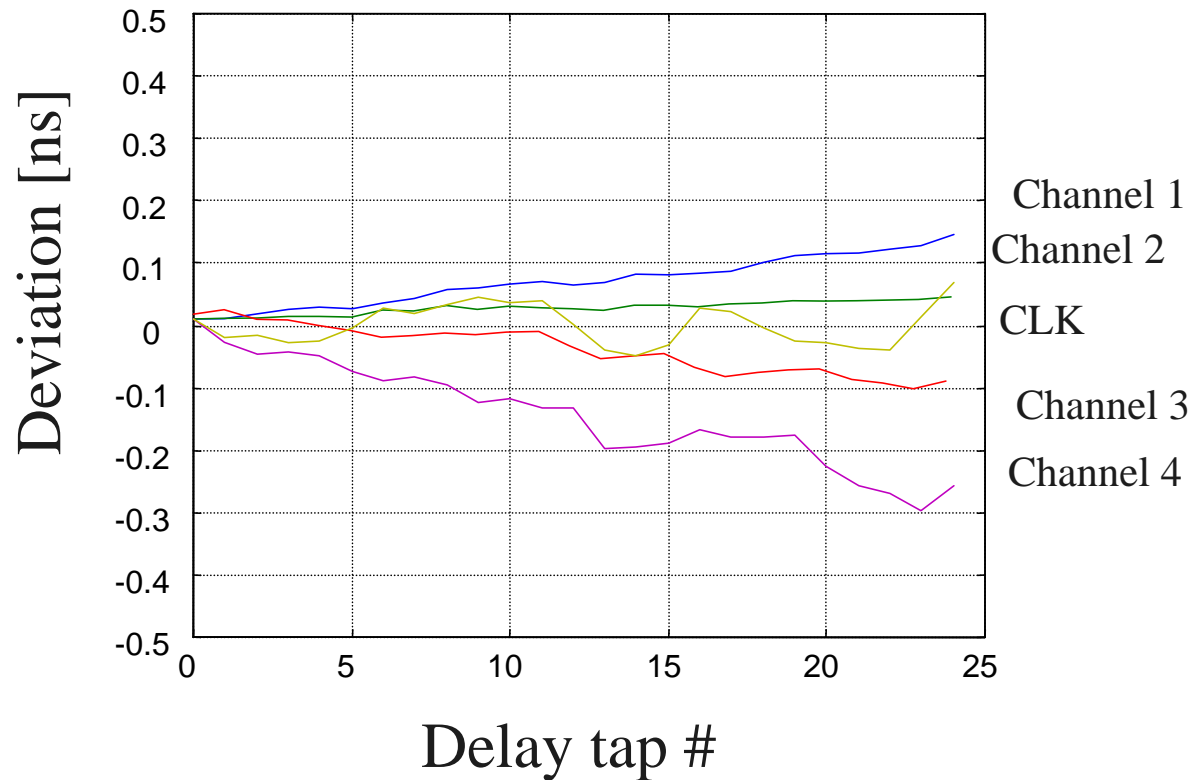
Jitter as a function of delay tap



Differential Nonlinearity



Integral Nonlinearity



Current consumption / channel

