
# LHCb and its electronics

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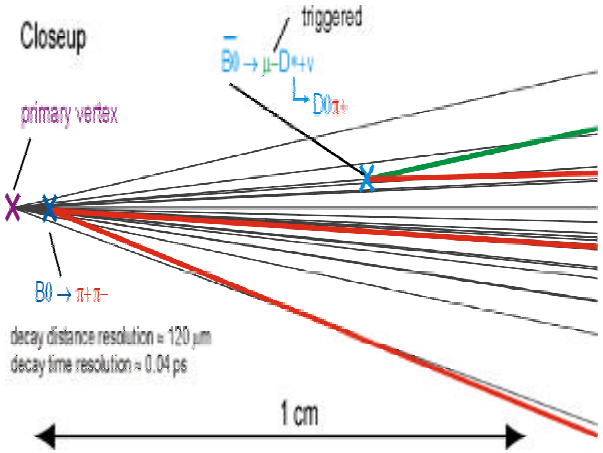
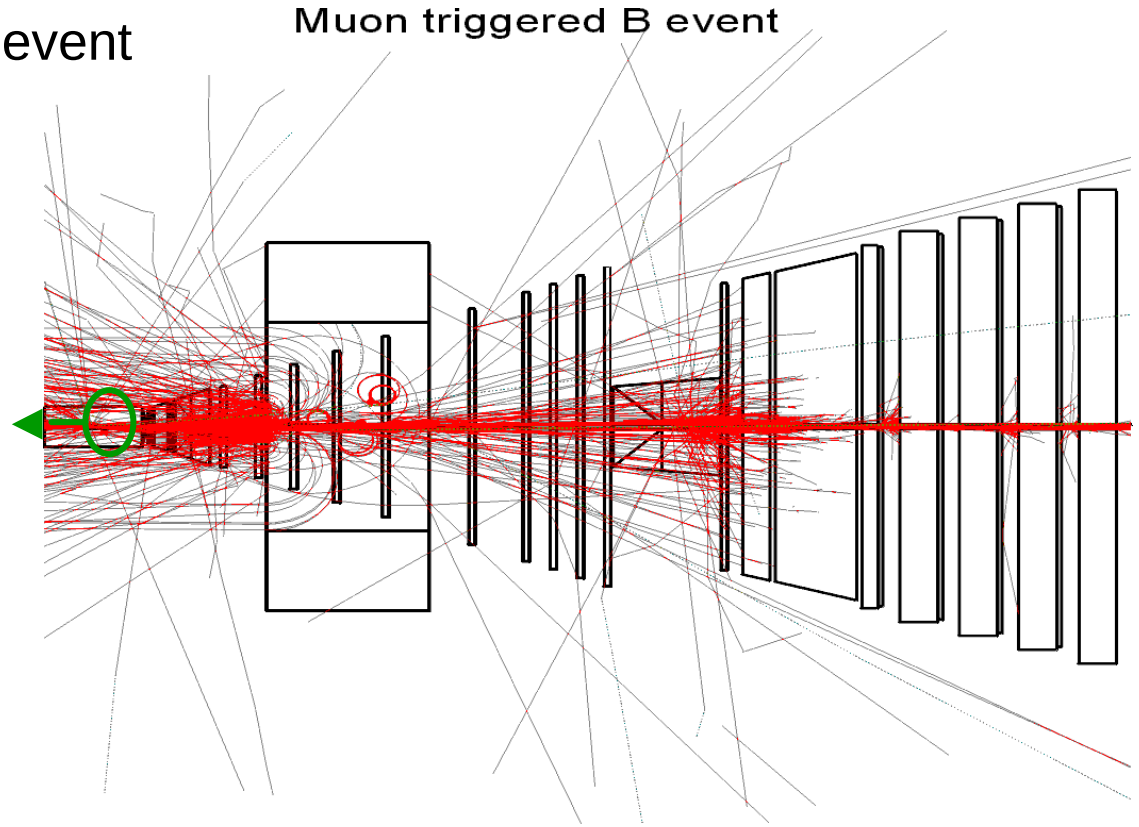
On behalf of the LHCb collaboration

# Physics background

- CP violation necessary to explain matter dominance
- B hadron decays good candidate to study CP violation
- B lifetime ~1ps -> short decay length (few mm)
- 40 - 400 tracks per event



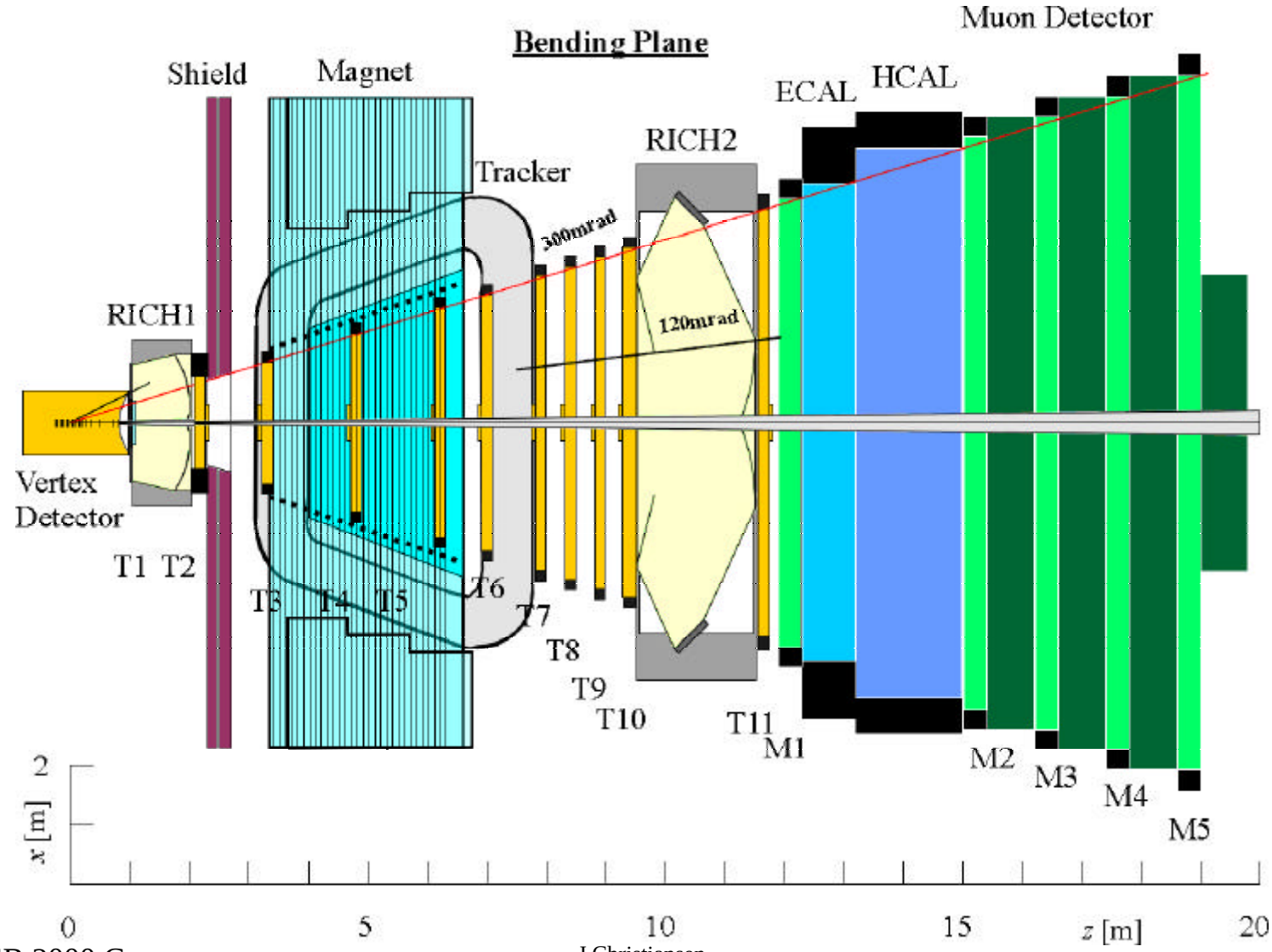
# LHCb differences from ATLAS/CMS

- ~1/4 size: budget, physical size, number of collaborators
- 1.2 million channels in 9 different sub-detectors
- Particle identification vital -> RICH detectors
  Vertex resolution vital -> Vertex detector in secondary machine vacuum
- Uses existing DELPHI cavern: reduced cost, must adapt
- Open detector with “fixed target topology” (easy access, sub-detectors mechanically “independent”, flexible assembly)
- Forward angle detector -> high particle density
- B physics triggering difficult -> 4 trigger levels with two in front-end
- One interaction per ~3 bunch crossings to prevent overlapping events in same crossing (ATLAS/CMS: factor ~50 higher)
- First level (L0) trigger rate of 1 MHz (ATLAS/CMS: factor 10 - 20 lower)
- Consecutive first level triggers supported (ATLAS/CMS: gap of 3 or more)
- First and second level trigger (L0 & L1) buffering in front-end

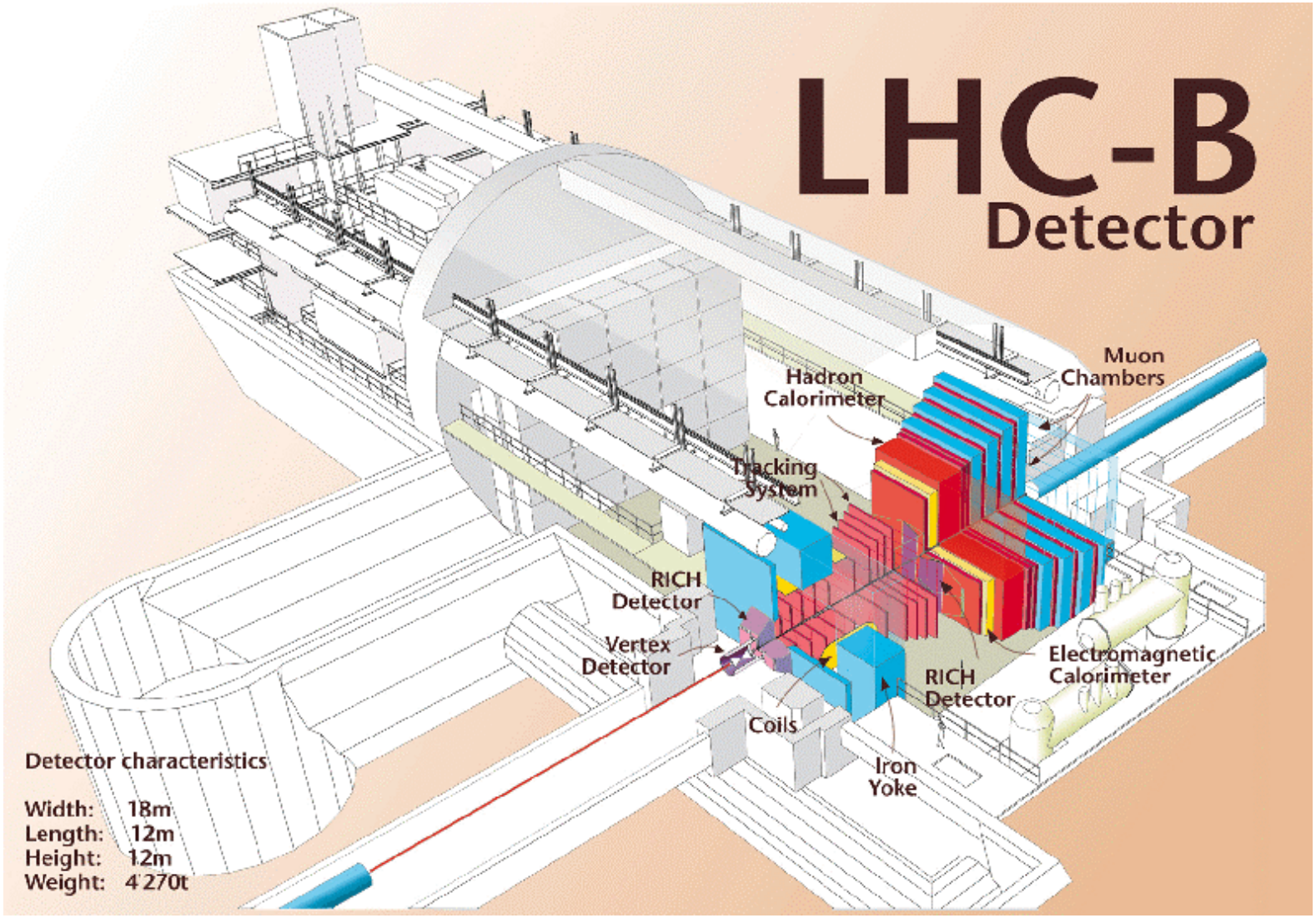
# LHCb evolution since LEB 97

- September 1998 LHCb approved
- General architecture maintained
- Most detector technologies now defined
- Key front-end parameters defined
- L0 latency 3 µs -> 4 µs
- L1 latency 50 µs -> 1000 µs (memory cheap)
- Buffer overflow prevention schemes defined:
- Front-end control defined (TTC, partitioning, overflow prevention, etc.)
- Electronics under development
- Better understanding of radiation environment (but more work needed)
- L2 and L3 trigger performed on same physical processor
- Architecture of trigger implementations defined
- Push architecture for DAQ event building network maintained
- Standard interface and data merger module to DAQ under design
- Start to make TDR's.

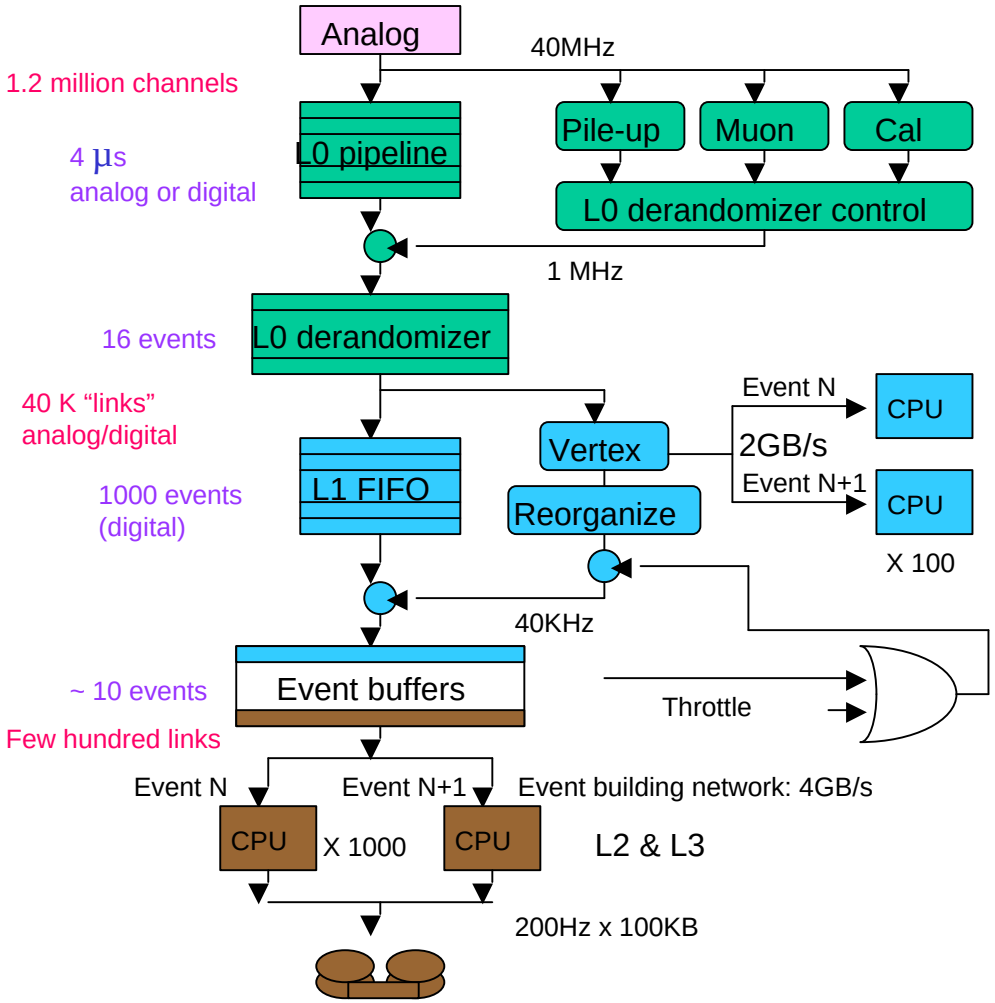
# LHCb sub-detectors



# LHCb detector in DELPHI cavern



# Front-end and DAQ architecture




Clock pipelined processing and buffering

Front-end simulated in VHDL

L1 trigger simulated in Ptolemy

Parallel processing in L1 trigger system
Event "pipelined" buffering in front-end

Front-end

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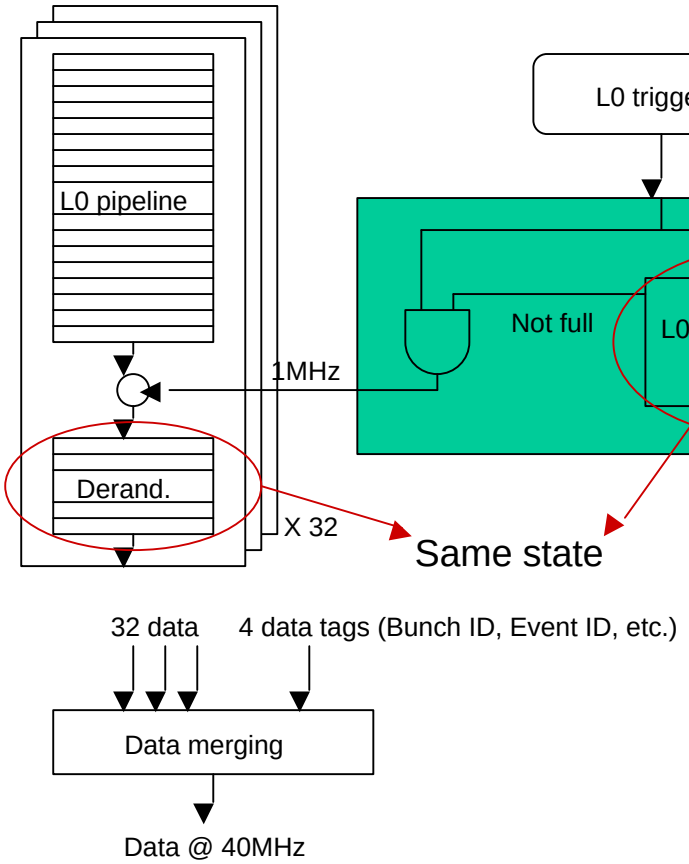
DAQ

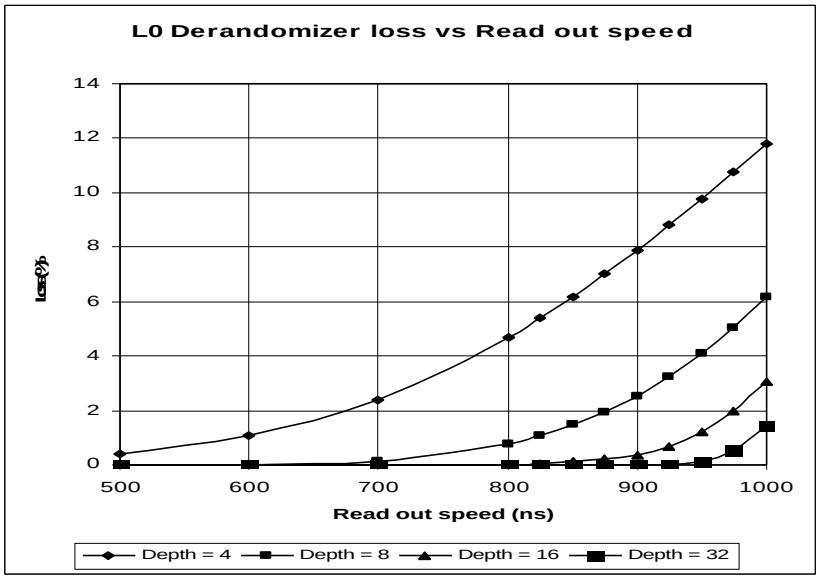
Parallel processing

# Front-end buffer control




Veto's all L0 trigger accepts that risk to overflow L0 derandomizers

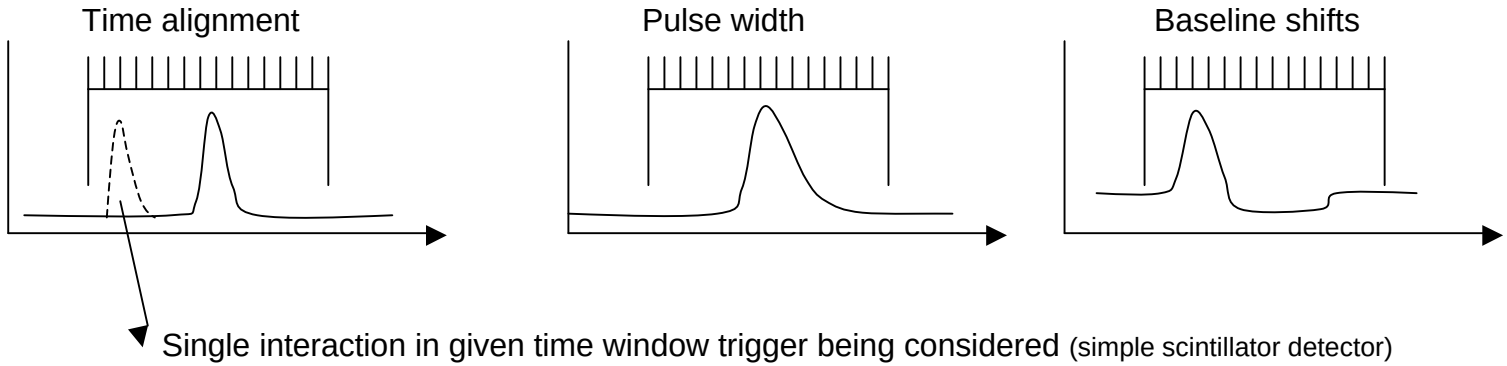
All L0 derandomizers must comply to given rule:
Minimum depth: 16 events
Maximum readout time: 900ns = (32+4)x25ns



# Consecutive L0 triggers

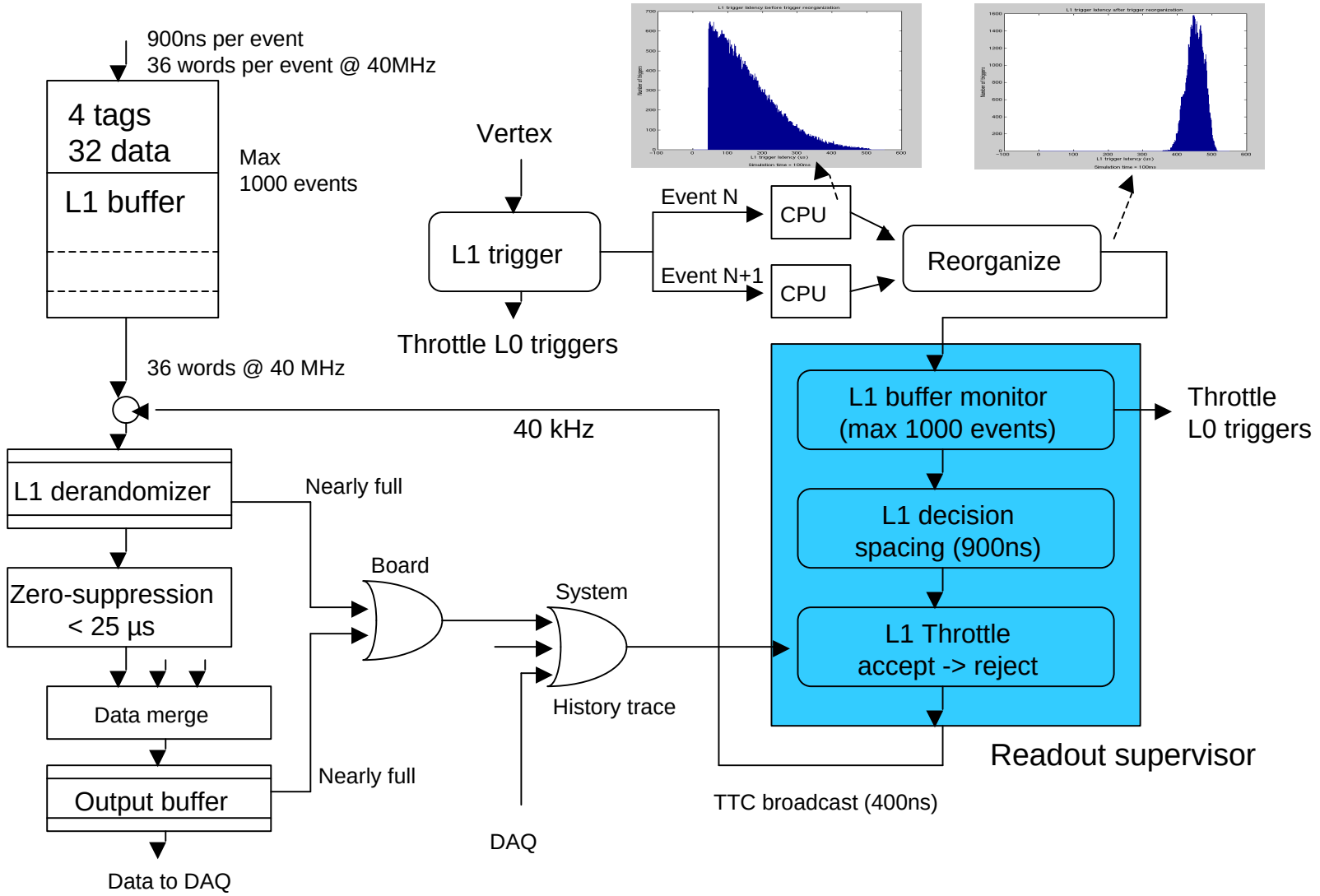
- Gaps between L0 triggers would imply ~3% physics loss per gap at 1MHz trigger rate.
- Problematic for detectors that need multiple samples per trigger or detectors with drift time.
  - All sub-detectors have agreed that this can be handled
- Very useful for testing, verification, calibration and timing alignment of detectors and their electronics

Max 16 consecutive triggers



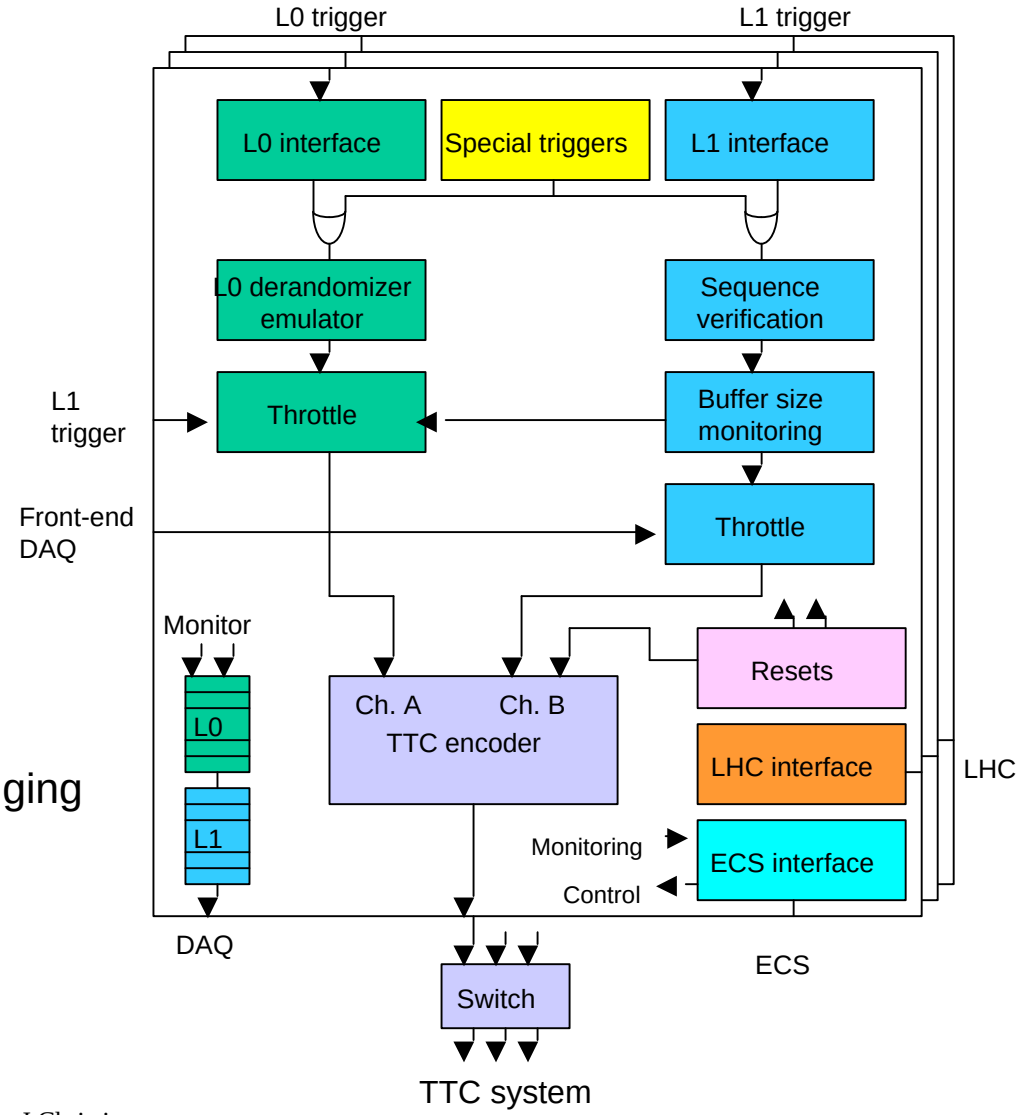

Single interaction in given time window trigger being considered (simple scintillator detector)
Use of single bunch mode of LHC machine being considered

# L1 buffer control

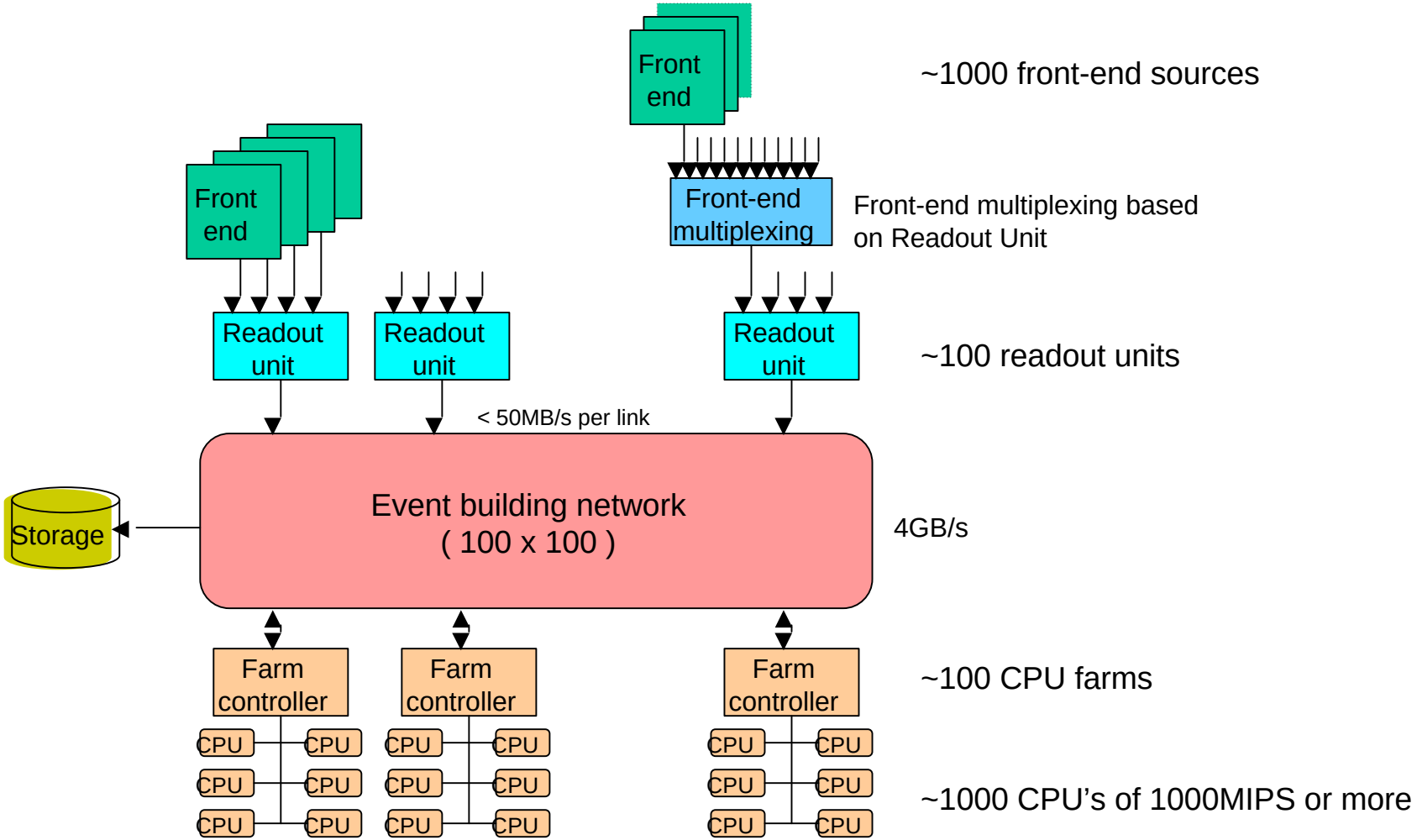


# Readout supervisor

- Main controller of front-end and input to DAQ
- Receive L0 and L1 trigger decisions from trigger systems.
- Restrict triggers to prevent buffer overflows in front-end, L1 trigger and DAQ
  - L0: Derandomizer emulation + Throttle
  - L1: Throttle
- Generate special triggers:
  calibration, empty bunch, no bias, etc.
- Reset front-end
- Drive TTC system via switch.
- Allow flexible partitioning and debugging
  - One readout supervisor per partition
  - Partitioning of throttle network
  - Partitioning of TTC system



# DAQ


Front end
Front end
Front-end multiplexing
Readout unit
Readout unit
Readout unit
< 50MB/s per link
Storage
Event building network
( 100 x 100 )
Farm controller
Farm controller
Farm controller
CPU
~1000 front-end sources
Front-end multiplexing based on Readout Unit
~100 readout units
4GB/s
~100 CPU farms
~1000 CPU's of 1000MIPS or more

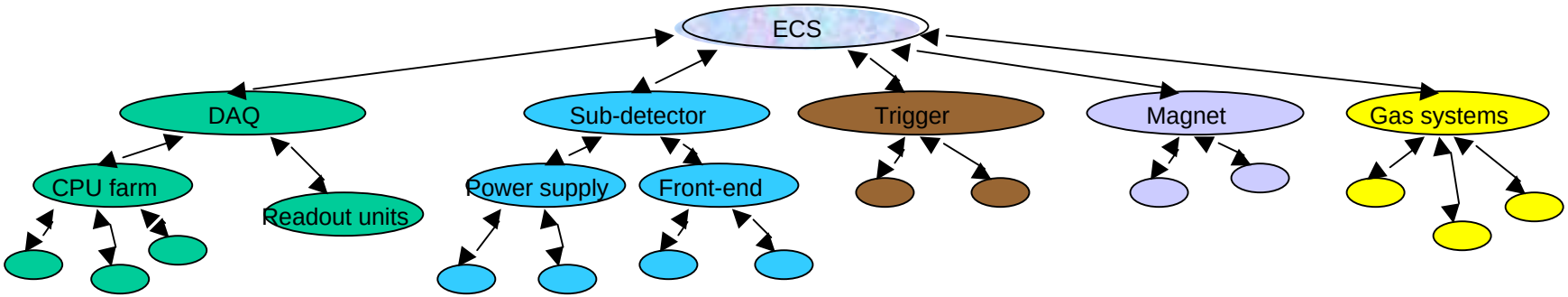
# Experiment control system (ECS)

## ECS controls and monitors everything in LHCb

- DAQ (partitioning, initializing, start, stop, running, monitoring, etc.)
- Front-end and trigger systems (initializing, calibration, monitoring, etc.)
- Traditional slow control (magnet, gas systems, crates, power supplies, etc.)

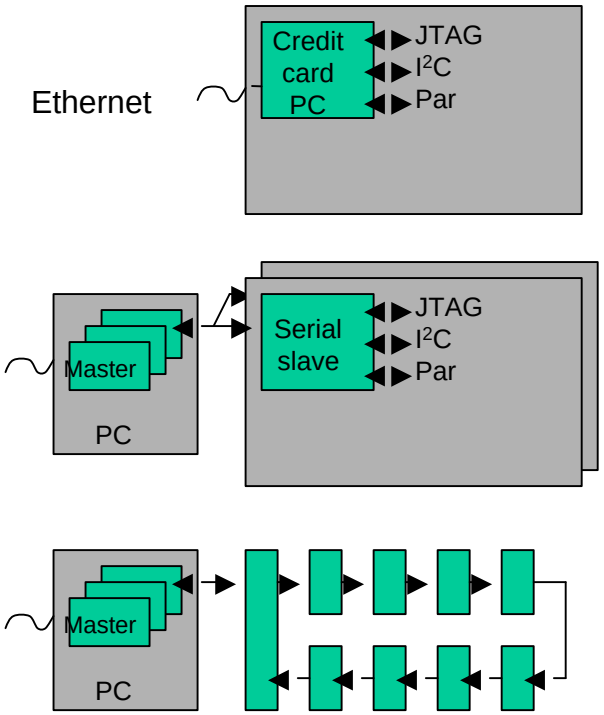
## Requirements

- Based on commercial control software (from JCOP)
- Gbytes of data to download to front-end, trigger, DAQ, etc.
- Distributed system with ~one hundred computers/processors.
- Partitioning into “independent” sub-systems (commissioning, debugging, running)
- Support standard links (Ethernet, CAN, etc.)



# ECS interface to electronics

- No radiation (counting room):
  Ethernet to credit card PC on modules
  Local bus: Parallel bus, $I^2C$, JTAG
- Low level radiation (cavern):
  10Mbits/s custom serial LVDS twisted pair
  SEU immune antifuse based FPGA interface chip
  Local bus: Parallel bus, $I^2C$, JTAG
- High level radiation (inside detectors):
  CCU control system made for CMS tracker
  Radiation hard, SEU immune, bypass
  Local bus: Parallel bus, $I^2C$, JTAG




# Support

- Supply of interface devices (masters and slaves)
- Software drivers, software support

# Radiation environment

In detector: 1K - 1M rad/year
- Analog front-ends
- L0 pipeline (Vertex, Inner tracker, RICH)

Repair: Few days to open detector

Edge of detector and in nearby cavern:

Few hundred rad/year

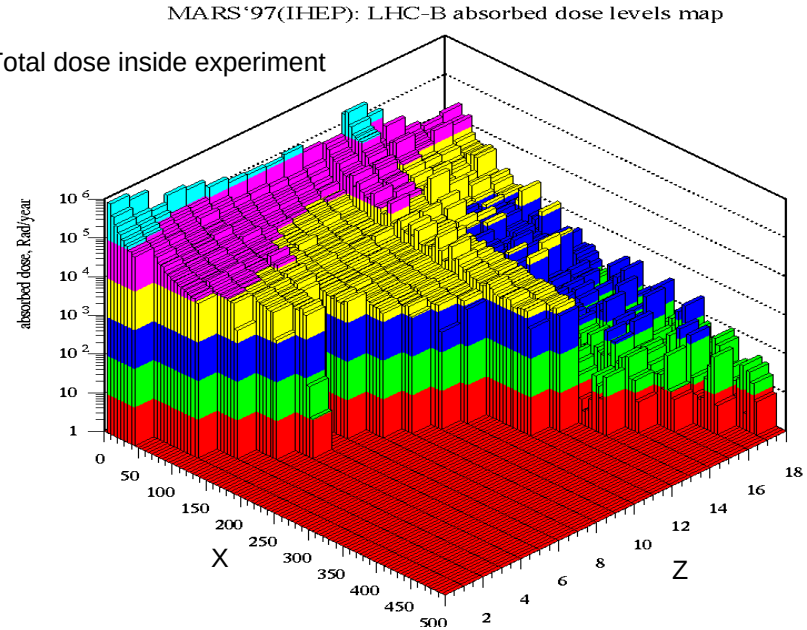
~ $10^{10}$ 1Mev neutrons/cm$^2$year
- L0 pipelines
- L0 trigger systems
- L1 electronics
- Power supplies ? (reliability)

SEU problems:
Control flip-flops
Memories
FPGA's

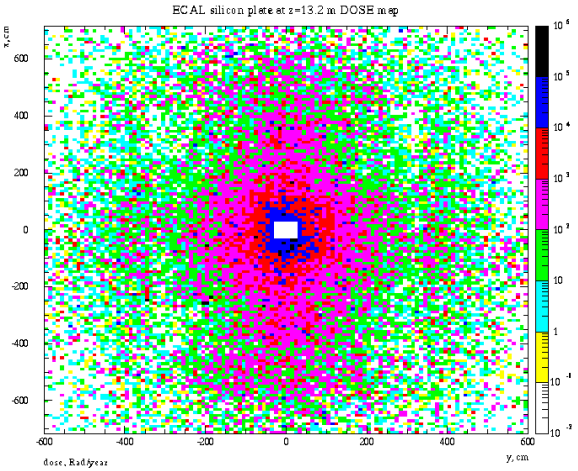
Access: 1 hour with 24 hour notice

Quick repairs must be possible
Remote diagnostics required

Total dose inside experiment




Ecal detector



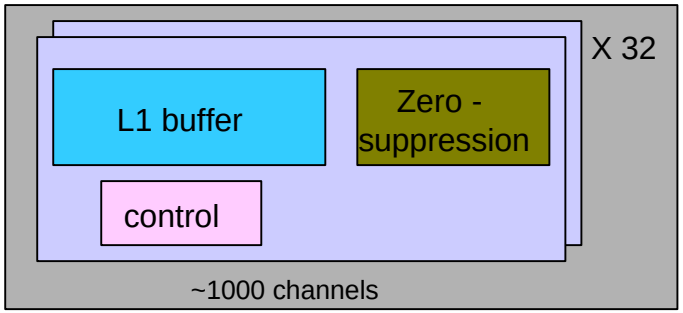
# Electronics in cavern

- Relatively low total dose
- Relatively low neutron flux

} Use of COTS justified

- Complex L0 trigger system and L0 and L1 electronics in cavern
  -> SEU becomes problematic

Typical L1 front-end board




Assumptions: Data memory not considered
32 FPGAs used for control & ZS
300 Kbit programming per FPGA
Total 10Mbits per board
1000 modules in total system

Hadron flux at edge of calorimeter: ~ 3 x $10^{10}$ part./$cm^2$/year, E > 10 Mev

Upset rate:

Xlinx

Module: 3 $10^{10}$ x 4 $10^{-15}$ x $10^{7}$=1200 per year (once per few hours)

System: 1200 x 1000 = 1.2 million per year (few per minute)

Recovery only by re-initialization !!.

# Errors

- Monitoring
  - Assume soft errors from SEU and glitches
  - All event fragments must contain Bunch ID, Event ID plus option of two more tags (error flags, check sum, buffer address, etc).
  - Errors in data “ignored”
  - Errors in control fatal:
    - All buffer overflows must be detected and signaled
      (even though system made to prevent this)
    - When merging data, event fragments must be verified to be consistent
    - Self checking state machines encouraged (one hot encoding)
    - Continuos parity check on setup parameters encouraged
- Recovery
  - Quick reset of L0 and L1 front-ends specified
  - Fast download of front-end parameters
  - Local recovery considered dangerous

# In-situ testing

- All registers must have read back
- Never mix event data and system control data
- Effective remote diagnosis for electronics in cavern to enable quick repairs (1 hour)
  - Sub-systems
  - Boards
  - Data links
  - Power supplies
- Use of JTAG boundary scan encouraged (also in-situ)

# ASIC's

- Needed for required performance
- Needed for acceptable cost (but ASIC's are expensive)
- Problematic for time schedules
  - 1 year delay in designs can easily accumulate.
  - Time for testing and qualification often underestimated.
  - Remaining electronics can not advance before ASIC's ready.
  - Design errors can not be corrected by "straps".
  - Technologies are quickly phased out in today's market (5 years).
  - Use of single supplier potentially dangerous.
- All sub-detectors rely on one or a few key ASIC's
- ASIC's in LHCb:
  - Designs: ~10
  - Total volume: ~ 50 K
  - Technologies: 4 x 0.25 µm CMOS, DMILL, BiCMOS, etc.
  - Prototypes of most ASIC's exist

We are a very small and difficult customer that easily risks to be put at the bottom of the manufactures priority list

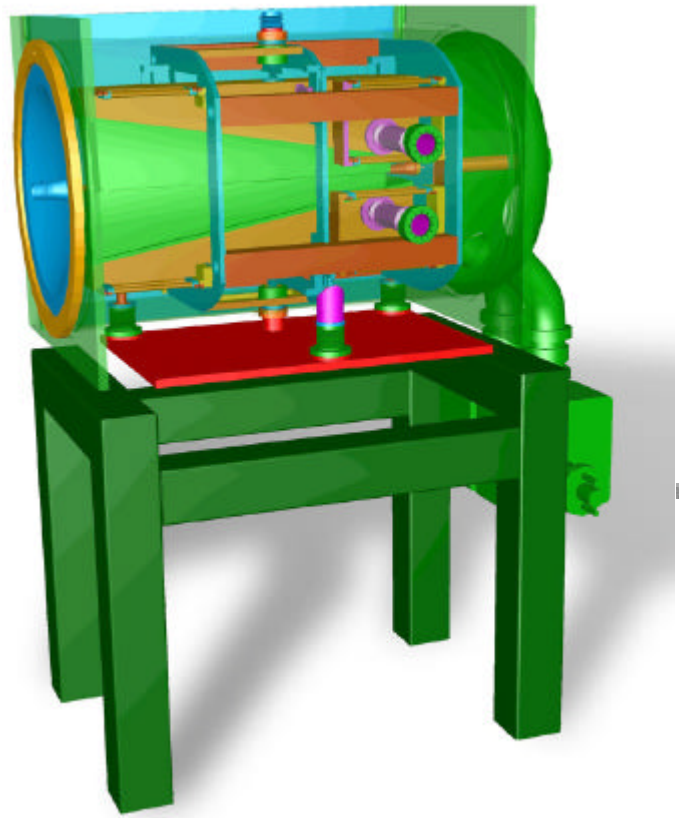
# Where are we now

- Progressing towards TDR's over coming year.
  Long production time -> now
  Short production time -> later
- Architecture and parameters of Front-end, trigger and DAQ systems defined.
- Working on prototypes of detectors and electronics.
- Ready to select ECS system
  Part of JCOP
  Standardizing ECS interfaces to front-ends.
- Event building network of DAQ not yet chosen
  Uses commercial technology which must be chosen at the latest possible moment to get highest possible performance at lowest prices
  (Gigabit Ethernet or alike)

# A few implementations

Vertex vacuum tank

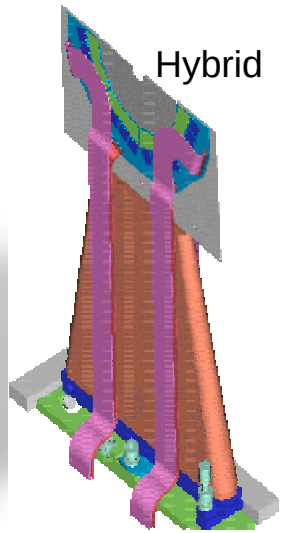
1.5 m



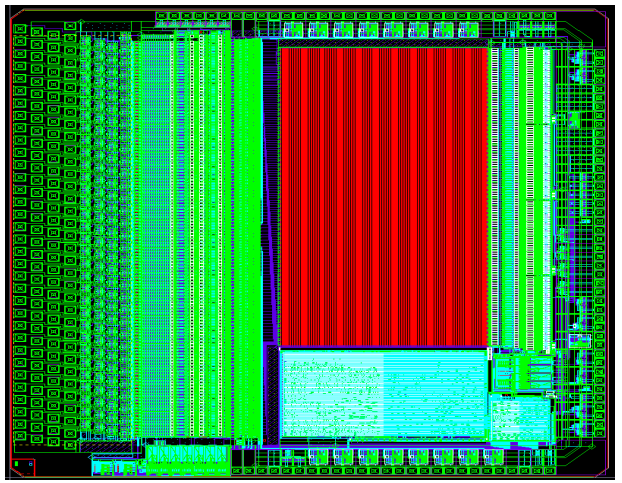
Used in 2 (3)
LHCb detectors

Backup in DMILL
(SCTA-VELO)

Hybrid

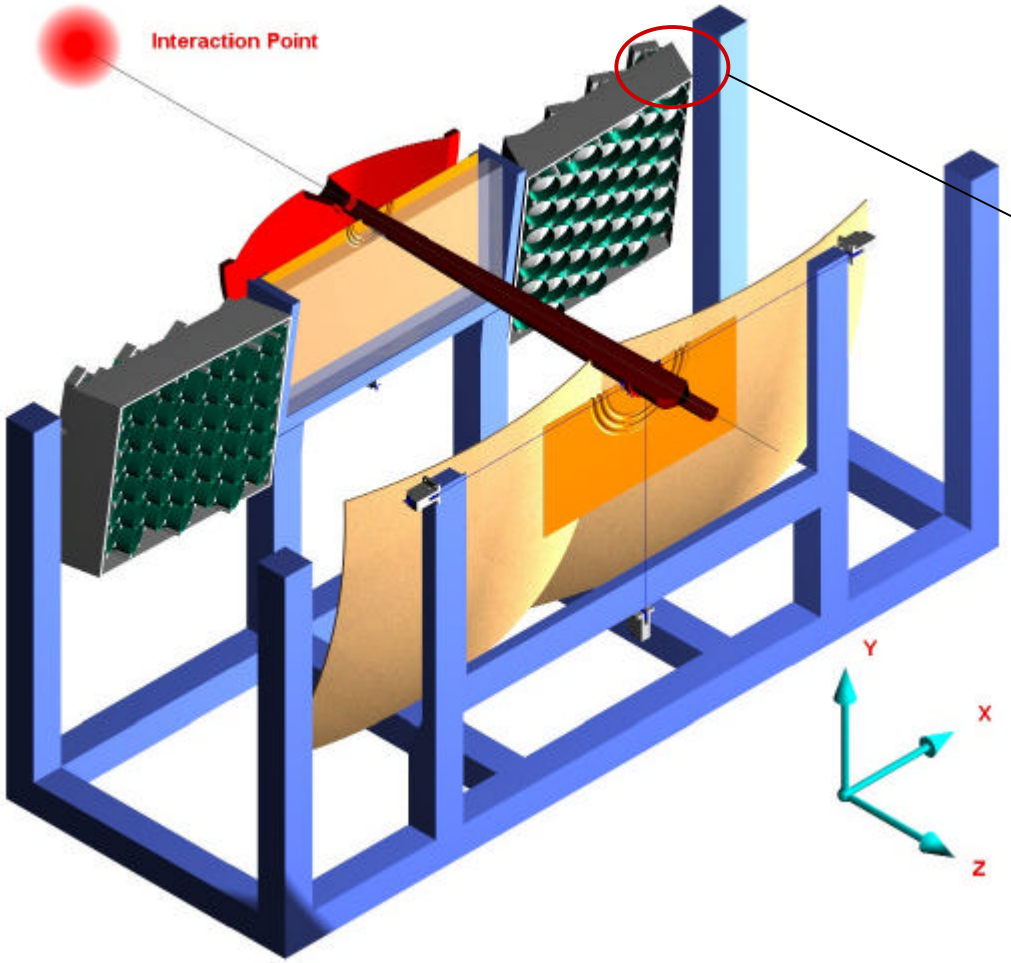


Beetle silicon strip front-end in 0.25 µm CMOS



Vertex detector prototype with SCTA front-end

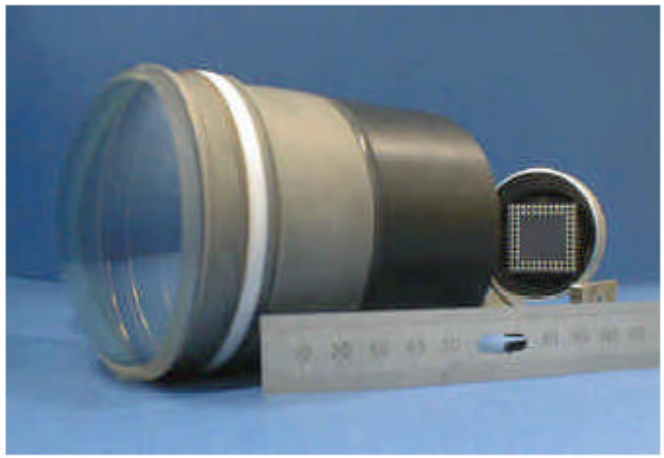
RICH detector




Pixel chip in 0.25 um CMOS is a common development with ALICE

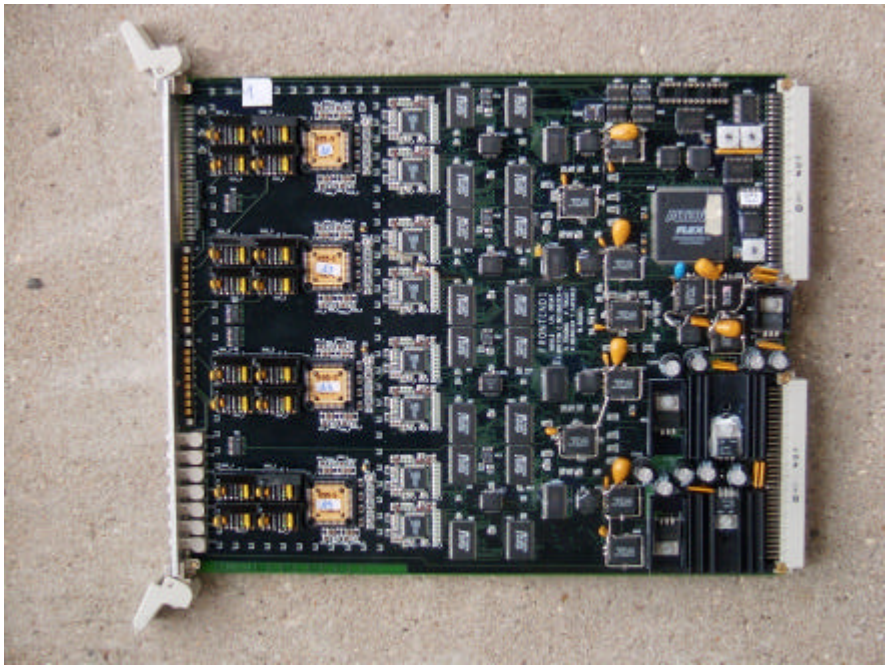
Critical time schedule as integrated into vacuum tube

Pixel Hybrid Photon Detector

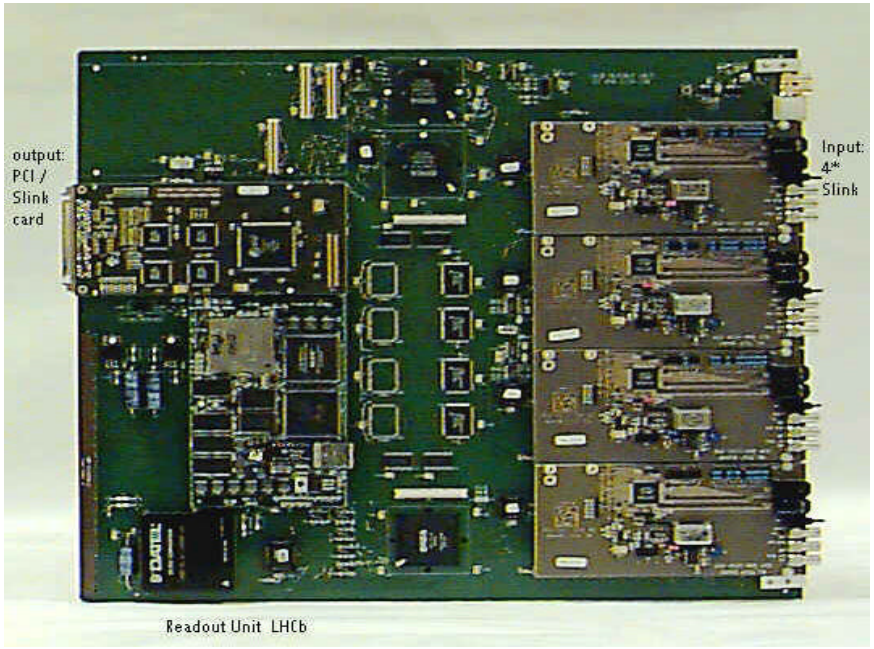


Backup solution using commercial MAPMT, read out by analog pipeline chip (Beetle or SCTA-VELO)

Hcal & Ecal 40 MHz 12bits front-end



Readout Unit: data concentration & DAQ interface



# LHCb electronics in numbers

| | | | | |
|---|---|---|---|---|
| Channels: | 1.2 million | | | |
| Sub-detectors: | 9 | | | |
| Triggers: | 4 | | | |
| Rates: | 1 MHz, | 40 kHz, | 5 kHz | 200 Hz |
| Latencies: | 4 us, | 1 ms, | 10 ms | 200 ms |
| Event size: | 100Kbyte | | | |
| ASIC's: | 50K in 10 different types | | | |
| TTCrx: | 2000 | | | |
| Data links: | 2000 optical + 40K short distance analog or LVDS | | | |
| 9U modules: | 1000 FE + 100 L0 + 100 RU + 50 control | | | |
| Racks: | 30 cavern, 80 underground counting room, 50 surface (DAQ) | | | |
| CPU's: | 100 L1 + 1000 DAQ + 100 ECS + FE DSP | | | |

# Electronics status

| System | FE architecture | Status | TDR |
|---|---|---|---|
| Front-end | Common definitions | Architecture and parameters defined | |
| L0 trigger | Pipelined | Architecture defined, Simulations | Early 02 |
| L1 trigger | Parallel CPU's | Architecture defined, Simulations + prototyping | |
| DAQ | Parallel, data push | Architecture defined, Simulations | Early 02 |
| Vertex | Analog readout | FE chip prototypes under test | Mid 01 |
| RICH | Binary pixel + backup | FE chip prototype to be tested | Sep 00 |
| Inner tracker | Same as Vertex | Defining detector type (substitute for MSGC) | End 01 |
| Outer tracker | ASD + TDC | Selecting ASD, TDC chip to be tested | Mid 01 |
| Preshower + E/H cal | Digital 10 bit<br>Digital 12 bit | FE prototypes tested | Sep 00 |
| Muon | Binary | Architecture + FE under study | Early 01 |

# Worries in LHCb electronics

- Time schedules of ASIC's may easily become critical
- Correctly quantify SEU problem in LHCb cavern
- Use of power supplies in LHCb cavern
- Support for common projects:
  TTC, radiation hard 0.25 um CMOS, power supplies, ECS framework
- Limited number of electronics designers available
  - Limited electronics support available from CERN
  - Limited number of electronics designers in HEP institutes
  - Difficult to involve engineering institutes/groups
    No funding for HEP electronics
    Prefer to work on industrial problems
    Prefer to work on specific challenges in electronics
    Hard to get electronics designers and computer scientists (booming market)
- Qualification/verification of ~10 ASIC designs, tens of hybrids and tens of complicated modules.
- Documentation and maintenance
- Supply of electronics components expected to become very difficult for small consumers in the coming two years

# Handling electronics in LHCb

- Electronics community in LHCb sufficiently small that general problems can be discussed openly and decisions can be reached.
- Regular electronics workshop of one week dealing with front-end, trigger, DAQ and ECS.
- Specific electronics meeting (1/2 day) during LHCb weeks with no parallel sessions to allow front-end, trigger, DAQ, ECS to discuss electronics issues.
- Electronics coordination part of technical board.
- It is recognized that electronics is a critical (and complicated and expensive and ----) part of the experiment.
- Review policy agreed upon (but not yet used extensively)
  Architecture, Key components (ASIC's, boards), Production readiness