An overview of the LHC-B experiment and its electronics

On behalf of the LHC-B collaboration

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Outline

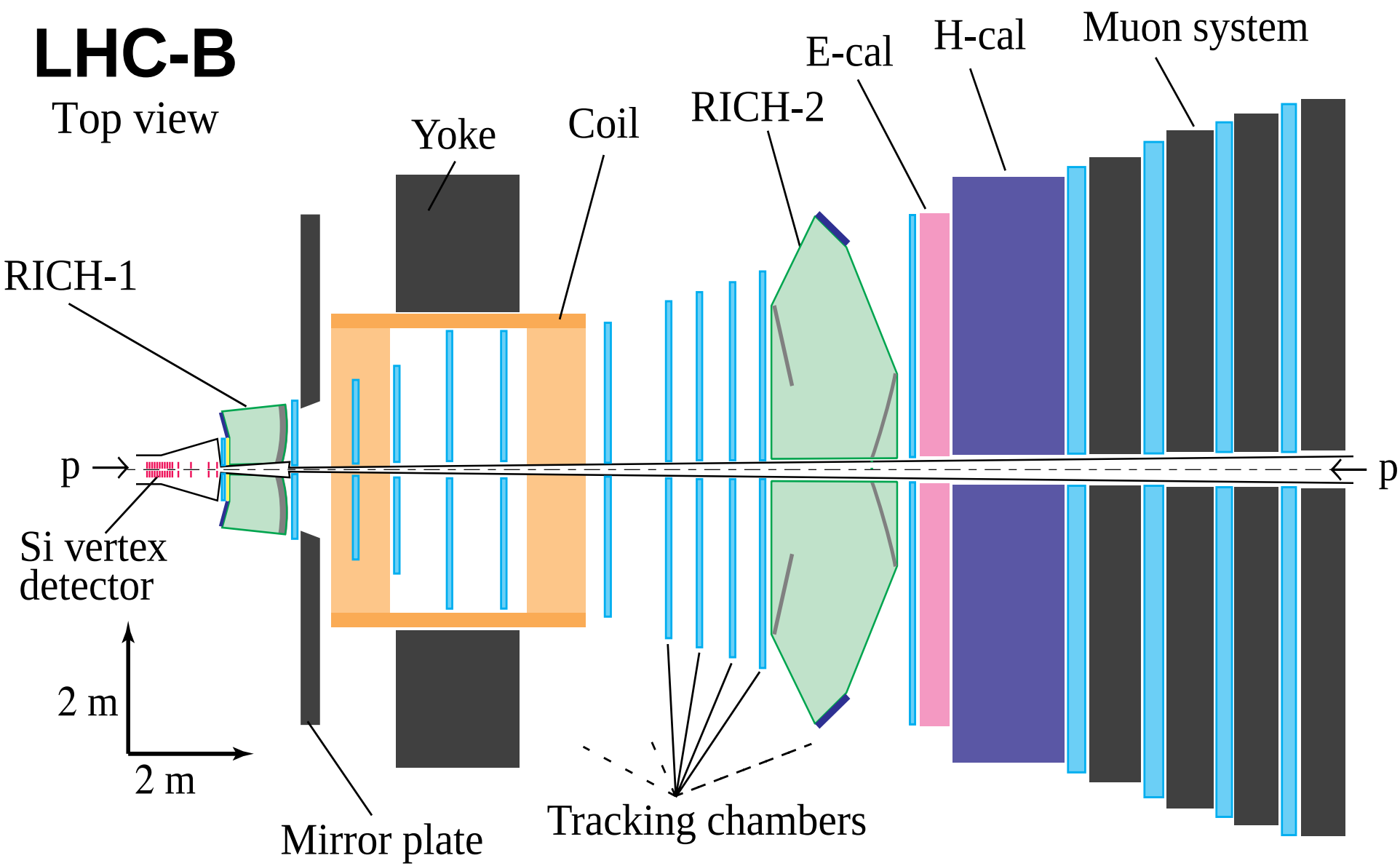
- LHC-B detector
- Trigger system
- Front-end electronics
- Data acquisition system
- Location of electronics
- Comparison to other major experiments
- LHC-B collaboration

LHC-B experiment

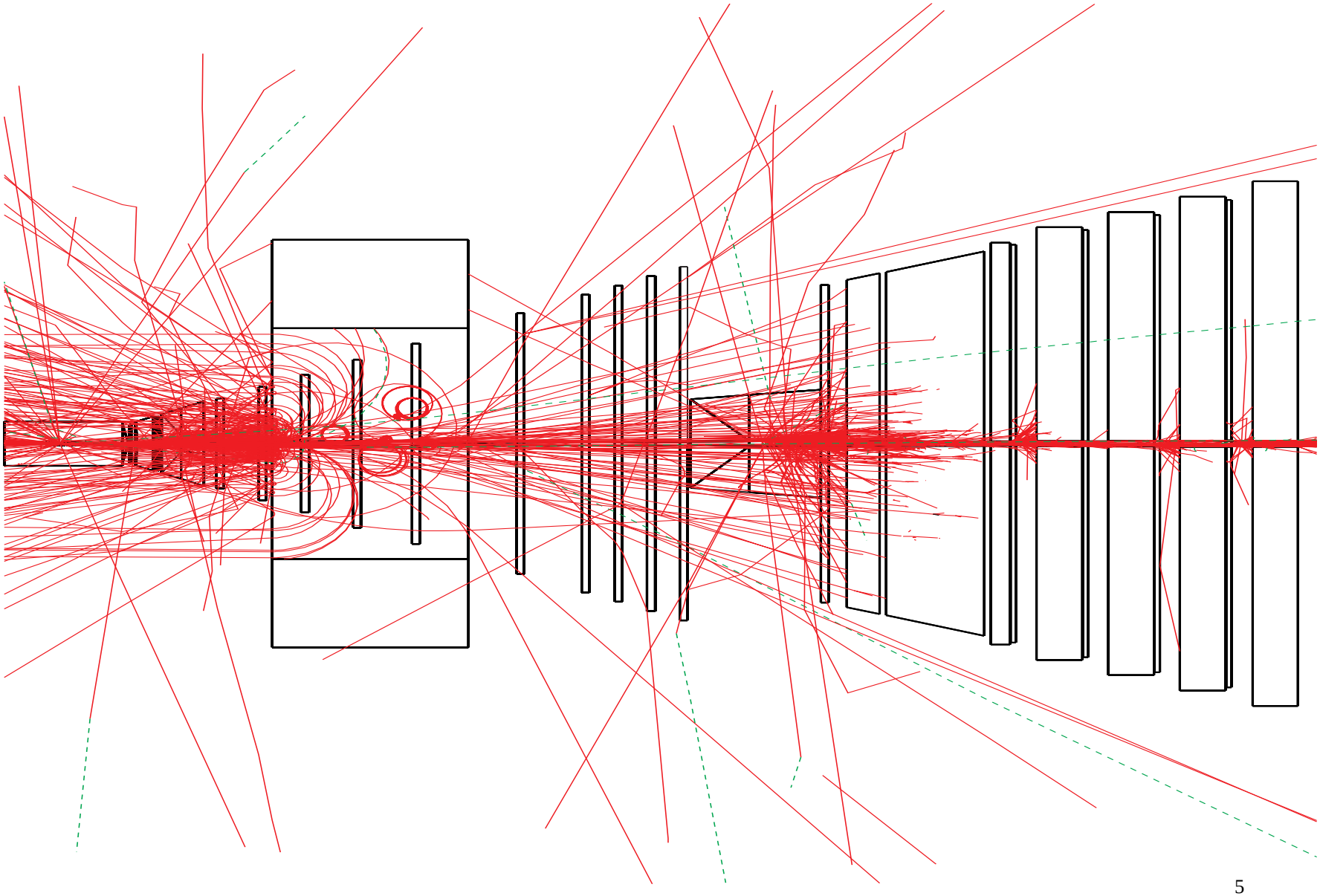
- Study of CP violation and rare phenomena in decays of Beauty particles.
- B hadron lifetime of a few pico seconds -> decay lengths of few millimeters.
  Makes it vital to identify primary and secondary vertex in trigger system.
- 15% geometrical acceptance of b final states in single arm detector covering forward angle between 10 mrad - 400 mrad (0.5 deg. - 23 deg.).
- Interaction rate limited to ~15 MHz to prevent multiple interactions and enable triggering system to identify b events of interest.
  LHC-B can run at full efficiency at start-up of LHC
- Charged particle rates in LHC-B follows a general $1/r^2$ dependency of radial distance to beam line.
  ~ 40 charged tracks in vertex and first tracker station
  ~ 350 charged tracks in last tracker station
- One million channels.
- Sophisticated triggering system to identify b events.
- Detector size comparable to typical LEP experiment.
- Located in DELPHI cavern with minimum civil engineering required.

LHC-B

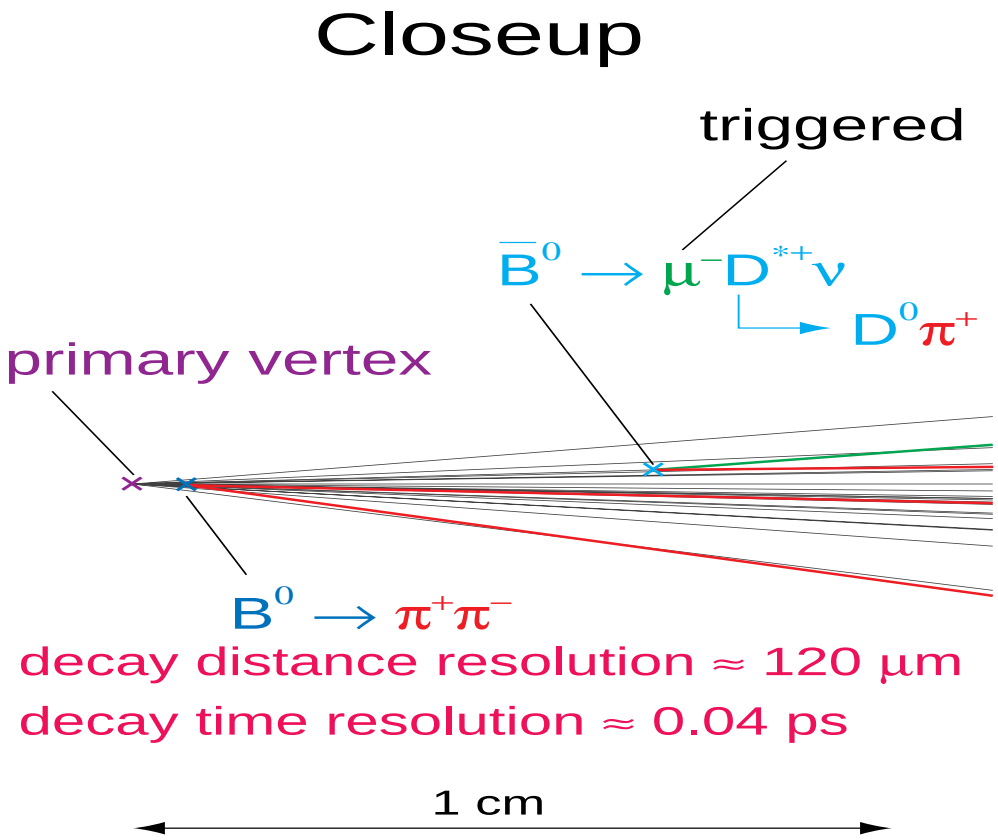
Top view

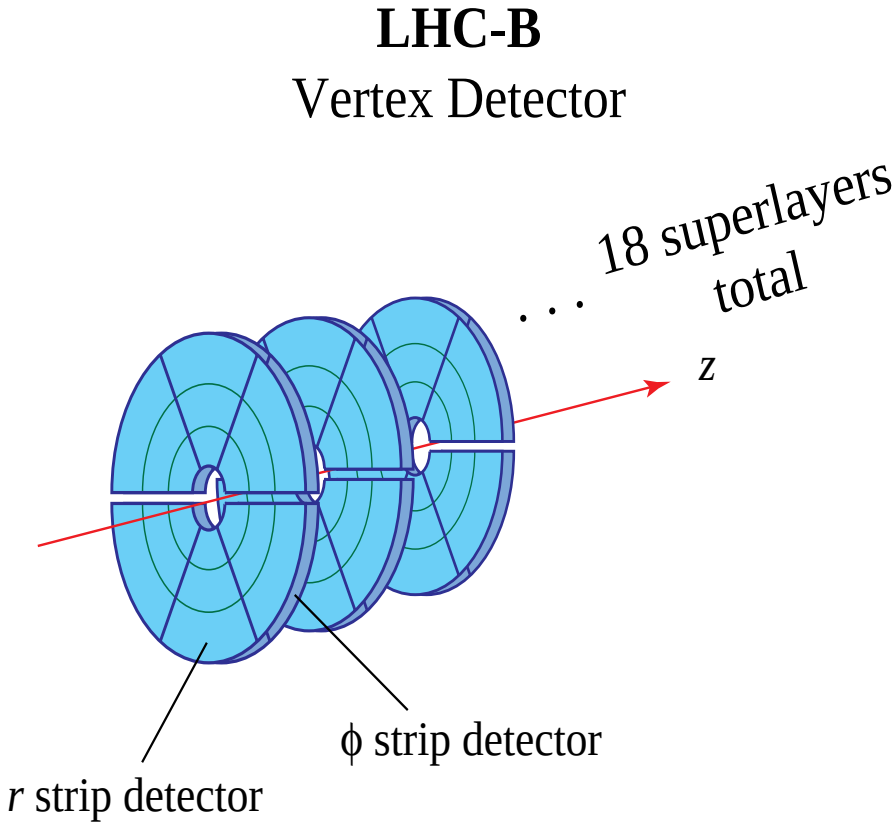


Muon triggered B events

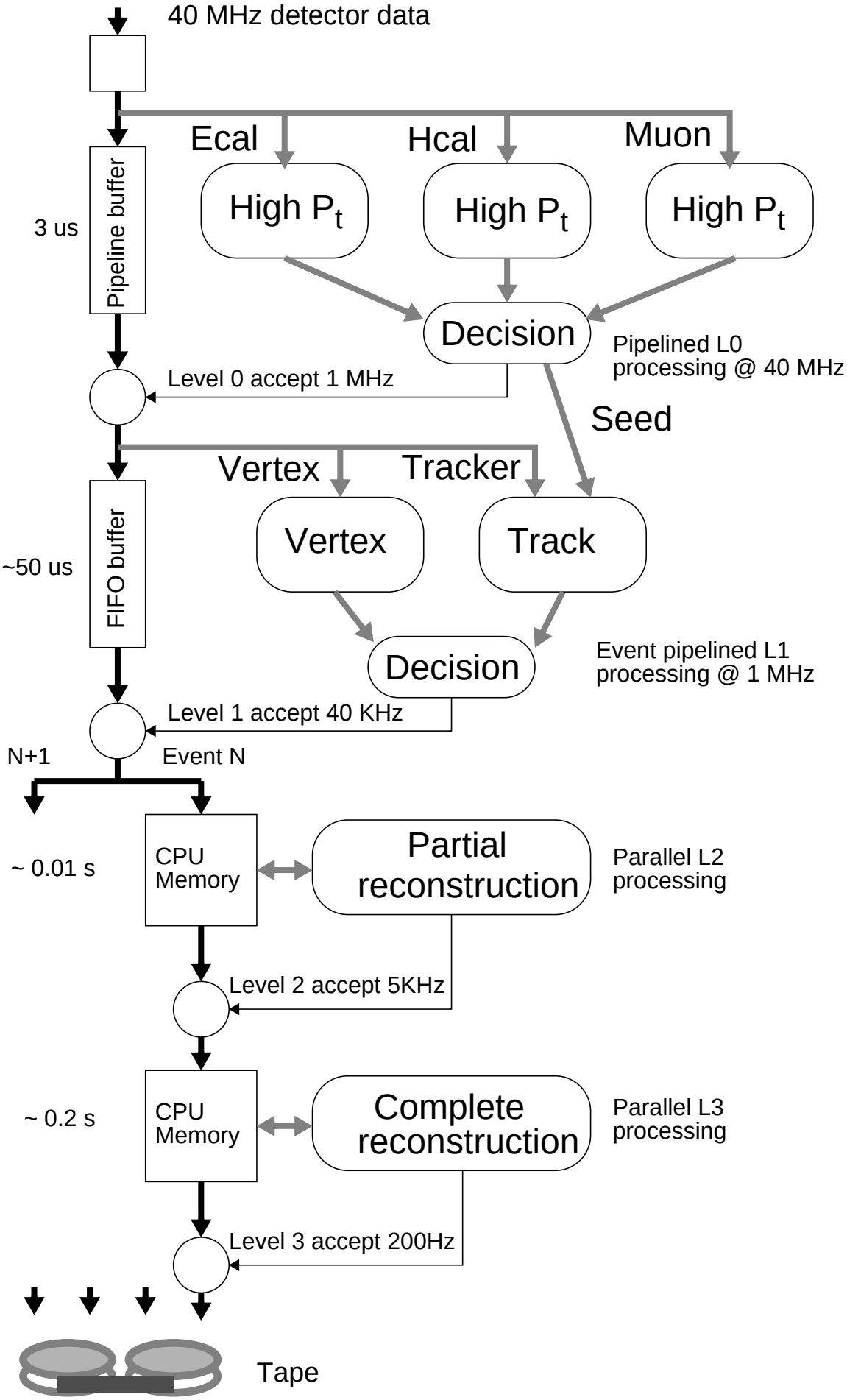


Micro vertex detector





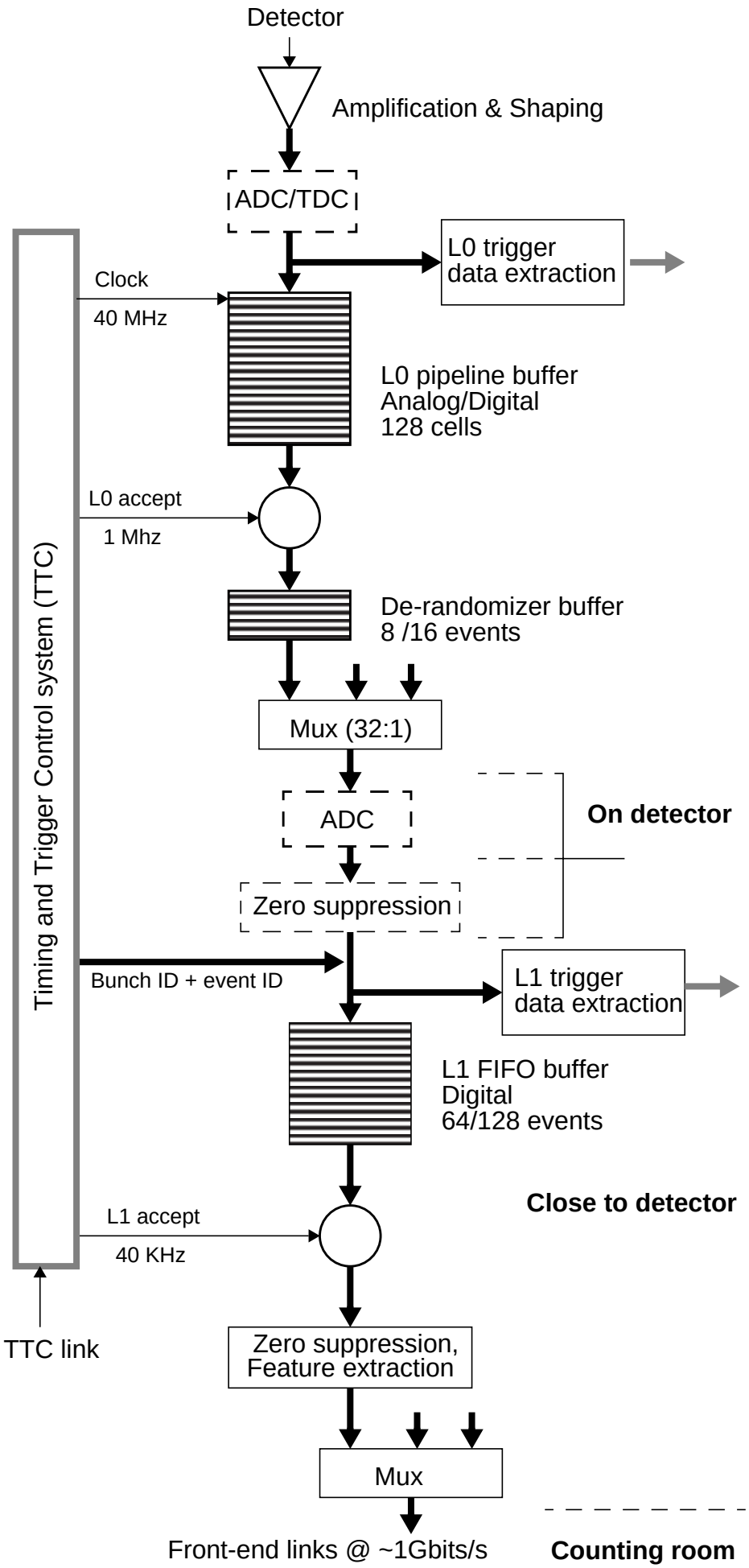
LHC-B trigger architecture



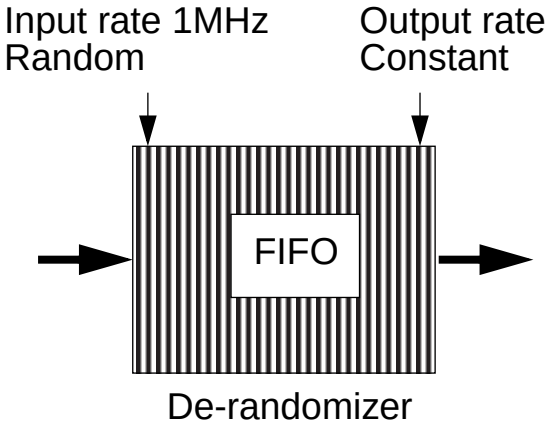
Trigger implementations in LHC-B

- Level 0
  - Clock pipelined @ 40 MHz
  - A: Hardwired using ASIC's + FPGA's
  - B: Programmable on array of special purpose processors (3D flow).
  - Centrally restrained to prevent buffer overflows.
- Level 1
  - Event pipelined @ 1 MHz
  - A: Hardware driven using FPGA's
  - B: Software driven farm of high performance processors.
  - A+B: Local processing in hardware + Global processing in processors.
  - Central supervisor delivering L1 decisions to front-end in correct sequence
- Level 2
  - Event parallel processing on ~400 processors
- Level 3
  - Event parallel processing on ~1000 processors

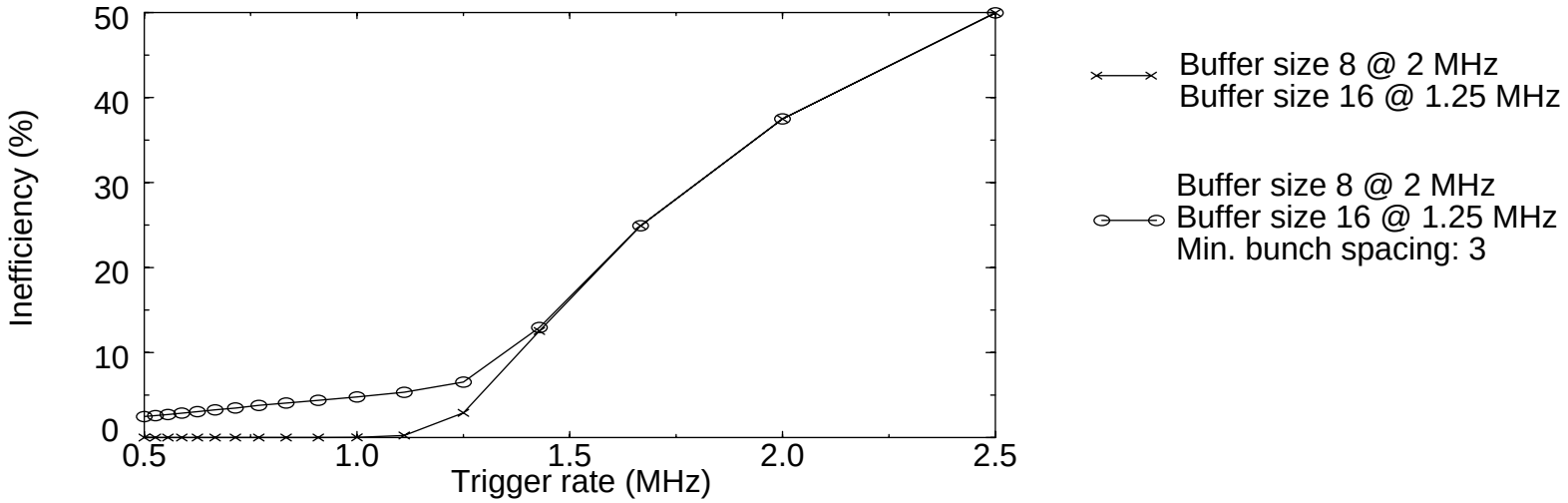
LHC-B front-end electronics



Trigger level 0 restrictions and de-randomizer buffer



Level 0 Inefficiency	Output rate / Input rate		
Buffer size	2	1.25	1
4	0.33%		
8	**0.003%**	0.6%	
16		**0.02%**	3.0%
32			1.5%
64			0.8%
128			0.4%



Minimum bunch spacing of 3 -> 5% dead time (0.5% for ATLAS, CMS)

Front-end electronics for level 0

- Pipelined L0 buffer:
  - Analog for detectors with large channel count and limited dynamic range.
    (Vertex, RICH, Inner tracker)
  - Digital for detectors with: limited channel count, large dynamic range, binary data, TDC data.
    (Calorimeters, Outer tracker, Muon)
- L0 derandomizer buffer
  - Centrally restrained L0 trigger to prevent buffer overflows.
  - 8 events if read-out at 2 MHz.
  - 16 events if read-out at 1.25 MHz. (32 channels multiplexed to 40 MHz ADC)
- Optional zero suppression to reduce data volume.
- Multiplexing to reduce number of cables.
- Clock and L0 trigger distributed by TTC system.
- Located on detector.

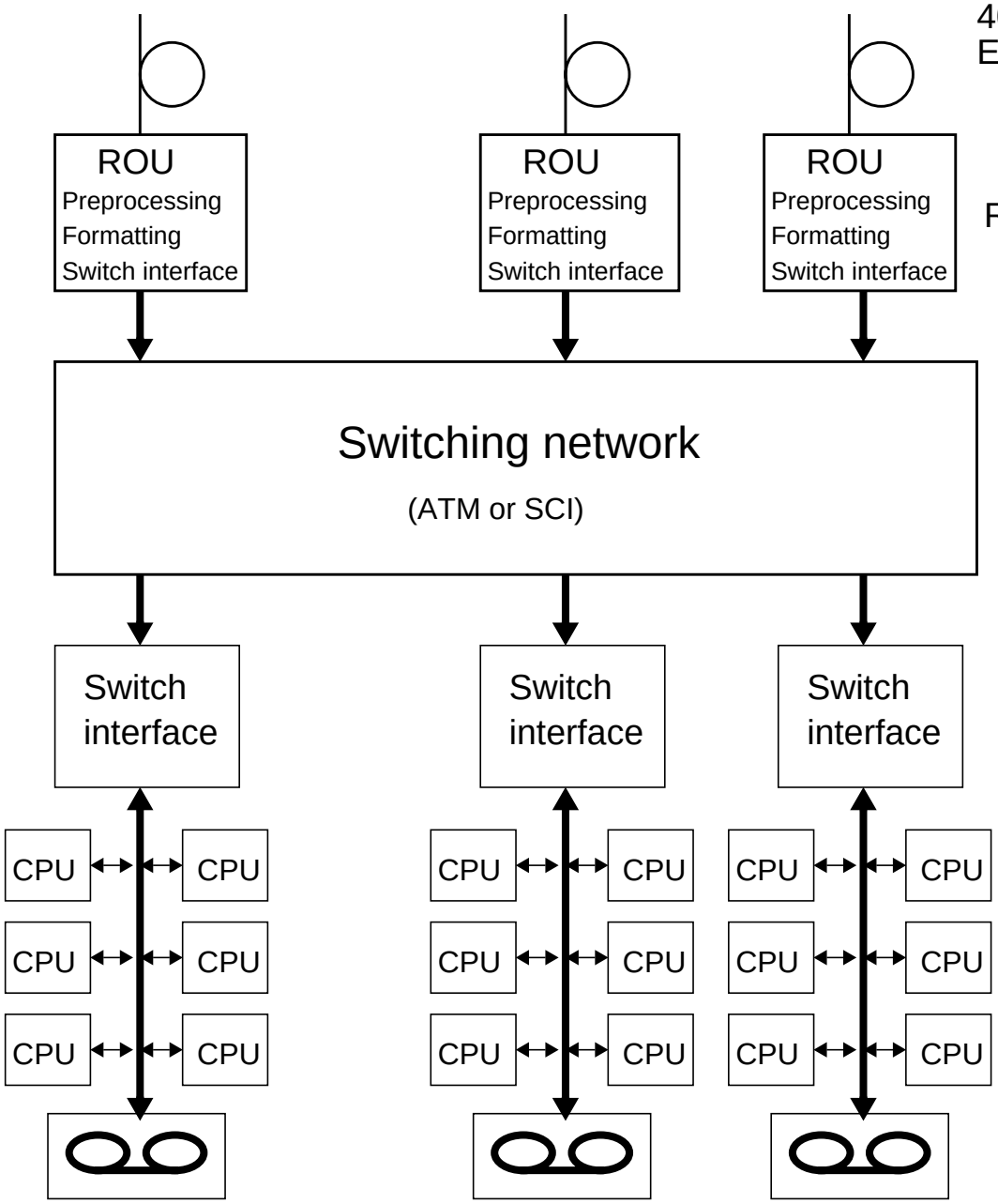
Front-end electronics for level 1

- All data digitized before level 1 buffer.
- L1 buffer implemented as Digital FIFO with event separators.
- L1 buffer implemented using commercial memory devices (DRAM).
- L1 buffer controller common to whole experiment (FPGA or ASIC).
- Width of L1 buffer detector dependent.
- L1 trigger decision distributed by TTC broadcast.
- L1 trigger decisions de-randomized before TTC system.
- Zero suppression and feature extraction of accepted L1 data.
- Formatting of event data.
- Multiplexing into limited number of read-out links (e.g. 1 Gbits/s).
- Located close to detector (few meters)

LHC-B DAQ system

100 - 200 Front-end links @ 1 Gbits/s

40 K events/s
Event size = ~100Kbyte



ROU= Read-Out Unit

1000 - 2000 CPU's of 1000MIPS

1/3 for L2 processing

2/3 for L3 processing

DAQ system

- A: Data sources push all event data to destination processor.
  - Events allocated to predefined processor or allocated by DAQ supervisor.
  - All event data sent to destination processor.
  - Large bandwidth required for event building network. (4 Gbytes/s)
  - Simple protocol handling.
  - Simple read-out units.
  - Automatic event assembly required in destinations.
- B: Partial read-out of data for Level 2 processing.
  - Detectors participating in L2 trigger sends data to processor.
  - Other detectors store L2 data in read-out units.
  - L2 reject clears L2 buffer in read-out unit.
  - L2 accept requests remaining data for L3 processing.
  - Reduced bandwidth of event building network required (~ 40%).
  - Complicated protocol handling.
  - Intelligent buffering required in read-out units.
- Event building network.
  - A: ATM: Telecommunications, Serial @ 155 or 620 Mbits/s, Buffered switching nodes.
  - B: SCI: Computer bus, Shared memory mapped bus, parallel 0.5 - 2 Gbytes/s, Ringlets.
  - C: Others: Giga bit ethernet, Myrinet, etc.

- Processors.

  Standard high performance processor year 2002 - 2004.

  ~1000 MIPS.

  1- 10 Gbyte memory

  High performance and intelligent network interface.

Location of electronics

- In detector: Analog front-end + level 0 pipeline
  - Distance: ~ cm
  - Electronics: Radiation hard or radiation tolerant
    - Radiation levels:
      - 10 cm ~200 Krad/year
      - 30 cm ~20 Krad/year
      - 100 cm ~2 krad/year
      - 300 cm ~0.2 Krad/year
  - Accessibility: Detector open (yearly)
- Close to detector: Level 1 buffer + zero suppression + feature extraction
  Level 0 trigger processing
  Level 1 trigger processing
  - Distance: Few meters.
  - Electronics: Commercial. (Screened for reliability and radiation tolerance)
    - Radiation levels: << 1 krad/year (100 rad/year)
    - Magnetic field shielding
  - Accessibility: LHC stopped. (weekly)
- Counting room: DAQ system
  - Distance: ~ 25 meters
  - Electronics: Commercial.
  - Accessibility: LHC running. (daily)

LHC-B Compared to other experiments

- CMS & ATLAS:
  - Higher interaction rate (~ factor 20).
  - Full angle coverage.
  - Same bunch crossing rate (40 MHz).
  - Similar Level 0 (level 1) latency.
  - Level 0 accept rate factor 10 lower.
  - Closed detector.
  - **Front-end electronics must be modified to accommodate 1 MHz L0 accept.**
- Hera-B
  - Similar interaction rate and track density
  - 10 MHz bunch crossing rate.
  - **Front-end electronics must be modified to 40 MHz bunch crossing rate.**

LHC-B collaboration

- ~45 Institutes
- ~300 physicists
- LHC-B collaboration requesting engineering resources for detector, electronics and software developments.
- LHC-B collaboration comparatively young and small.
- LHC-B collaboration currently working hard on finalizing technical proposal for spring 1998.

Key points for LHC-B electronics

- Use of commercial electronics in low (0.1 - 1 Krad/year) radiation level environments (VME crates with processors, FPGA's, power supplies, etc.)
- Radiation tolerant (10 - 100 K) electronics in commercial IC technologies.
- Feasibility of recovering pre-radiation functionality by annealing front-end electronics once per year (100 deg.cent for one week or equivalent).
- Accessibility of electronics located in detector cavern.
- Transmission of multiplexed analog data (8 bit) at 40 MHz on thousands of twisted pair cables over distances of ~10m (50m).
- Availability of (commercial) radiation tolerant 8 - 10 bit ADC's
- Availability of (commercial) radiation tolerant digital links.
- Ensuring that LHC-B benefits the most from front-end electronics developments in other LHC experiments.
- Use of common solutions and architectures in different sub detectors.
- Quality assurance (verification, testability, reliability)