General Outline

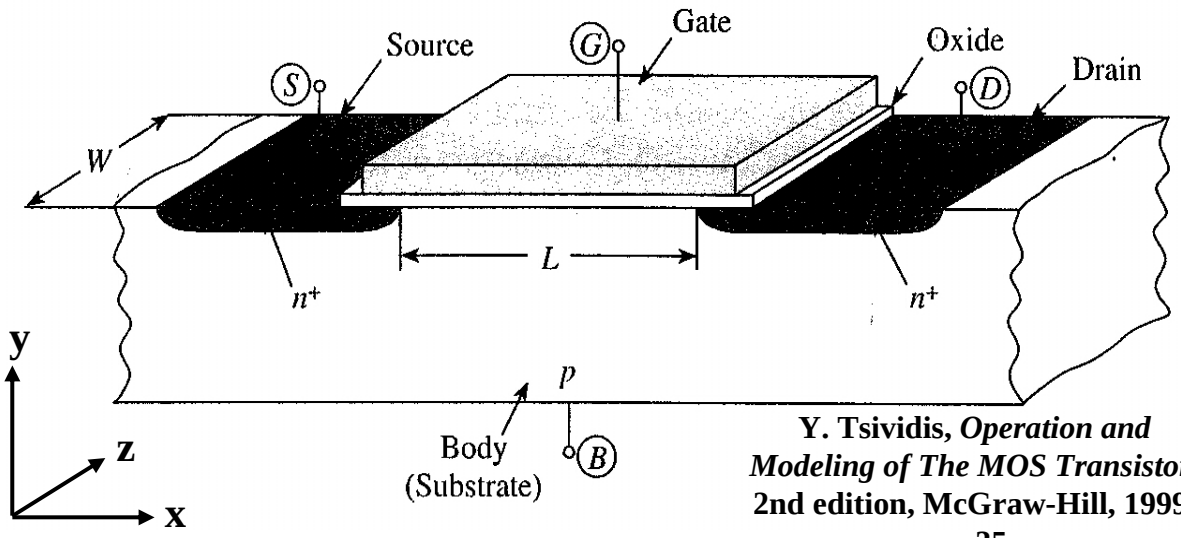
- ✓ ULSI technologies: manufacturing
- ✓ Radiation effects in devices and technologies
- ✓ Radiation Hardness-By-Design (HBD) techniques for ASICs
- ✓ 130nm technology node for High Energy Physics: vendor, properties, radiation effects

ULSI technologies: manufacturing

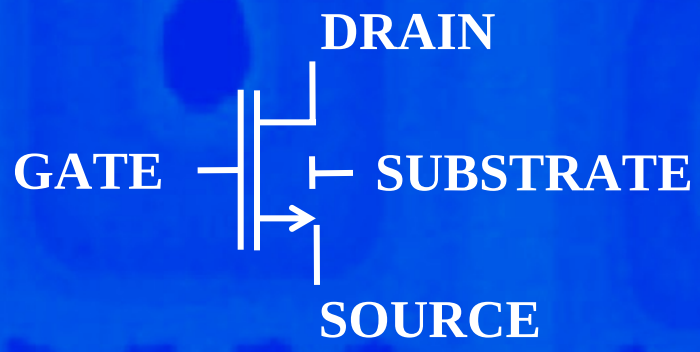
Outline

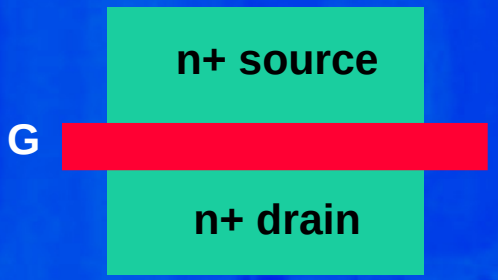
- ✓ Foreword
- ✓ Moore's law
- ✓ Manufacturing of ULSI CMOS technologies
  - Fundamental manufacturing operations
  - Process Flow
    - Front End Of Line (FEOL)
    - Back End Of Line (BEOL)

Foreword: the MOS transistor



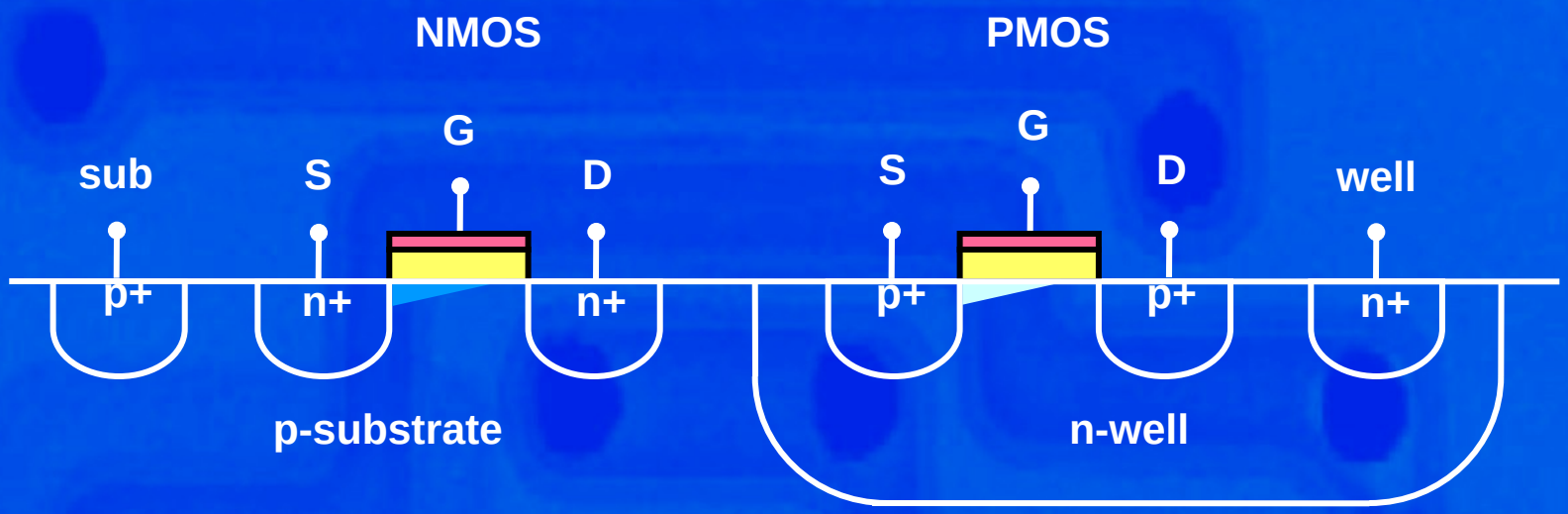
Y. Tsividis, *Operation and Modeling of The MOS Transistor*, 2nd edition, McGraw-Hill, 1999, p. 35

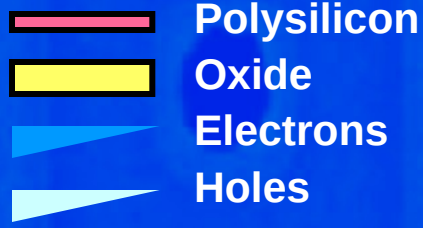


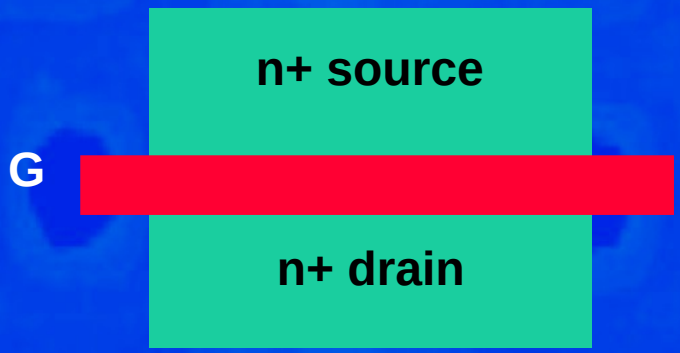


NMOS layout

Foreword: CMOS technology



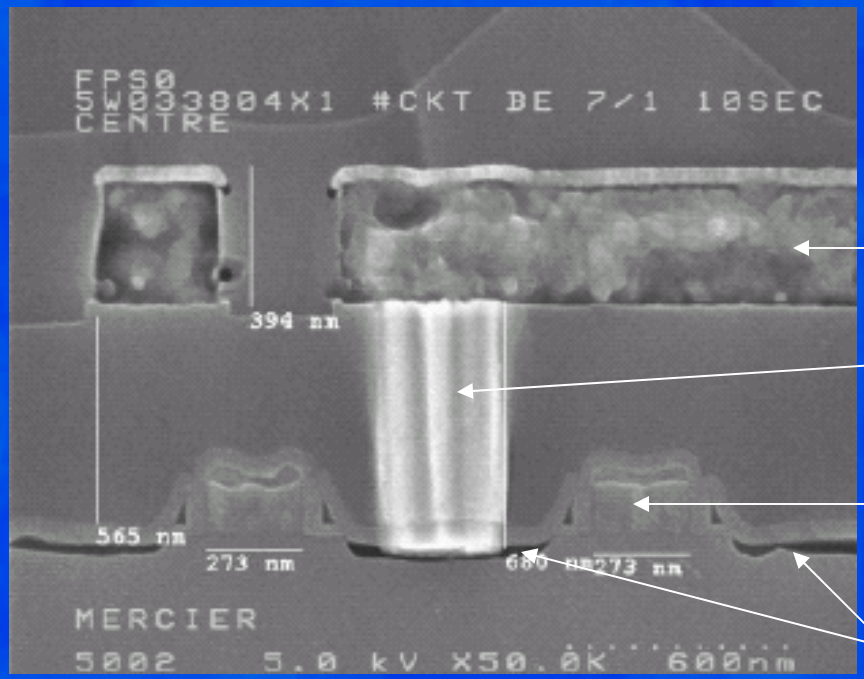




NMOS layout

Foreword: CMOS technology

- ✓ SEM (Scanning Electron Microscope) image of transistors



metal1

contact

polysilicon

silicide (source/drain)

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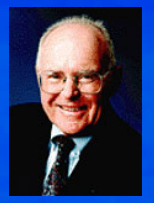
Moore's law



1965: Number of Integrated Circuit components will double every year

G. E. Moore, "Cramming More Components onto Integrated Circuits", *Electronics*, vol. 38, no. 8, 1965.

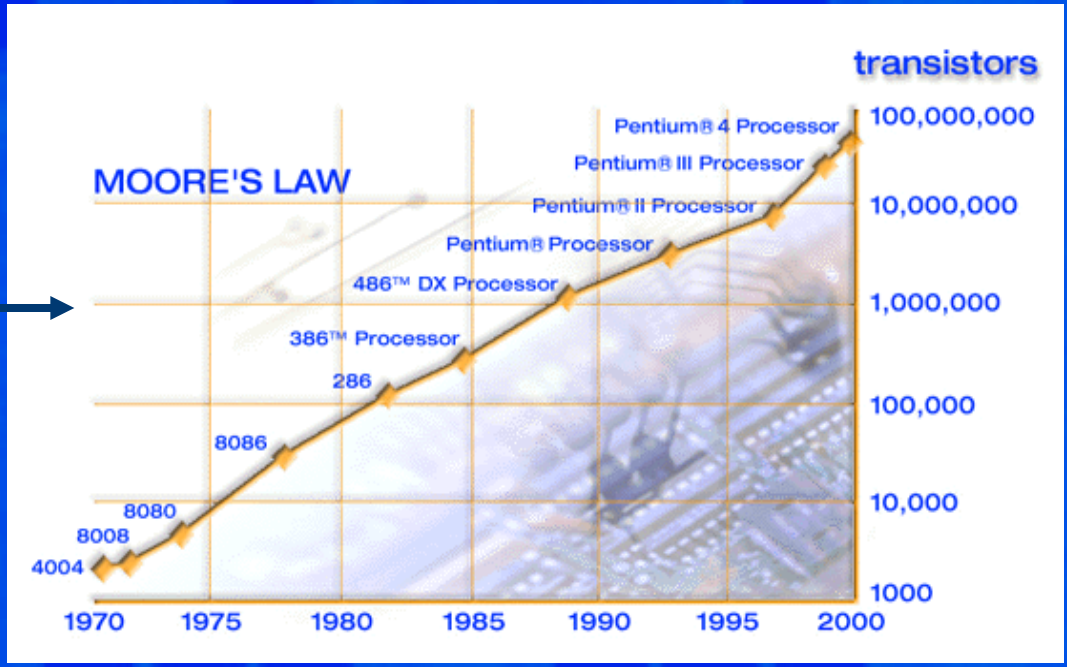
1975: Number of Integrated Circuit components will double every 18 months

G. E. Moore, "Progress in Digital Integrated Electronics", *Technical Digest of the IEEE IEDM 1975*.

1996: The definition of "Moore's Law" has come to refer to almost anything related to the semiconductor industry that when plotted on semi-log paper approximates a straight line. I don't want to do anything to restrict this definition. - G. E. Moore, 8/7/1996

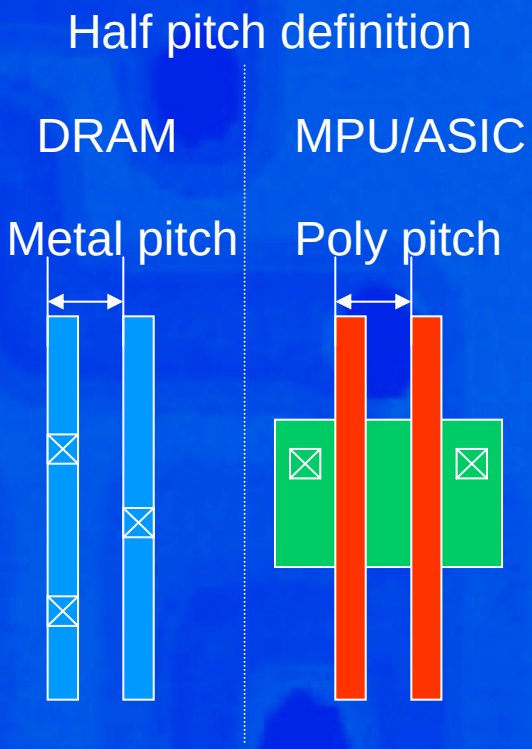
P. K. Bondyopadhyay, "Moore's Law Governs the Silicon Revolution", *Proc. of the IEEE*, vol. 86, no. 1, Jan. 1998, pp. 78-81.

An example:
Intel's Microprocessors



Moore's law fundamentals

- ✓ For every generation:
  - CD x 0.7
  - Area x 0.5
  - Chip size x 1.5
  - Structural improvement x 1.3
  - N of components x 4
  - Clock frequency x 1.4



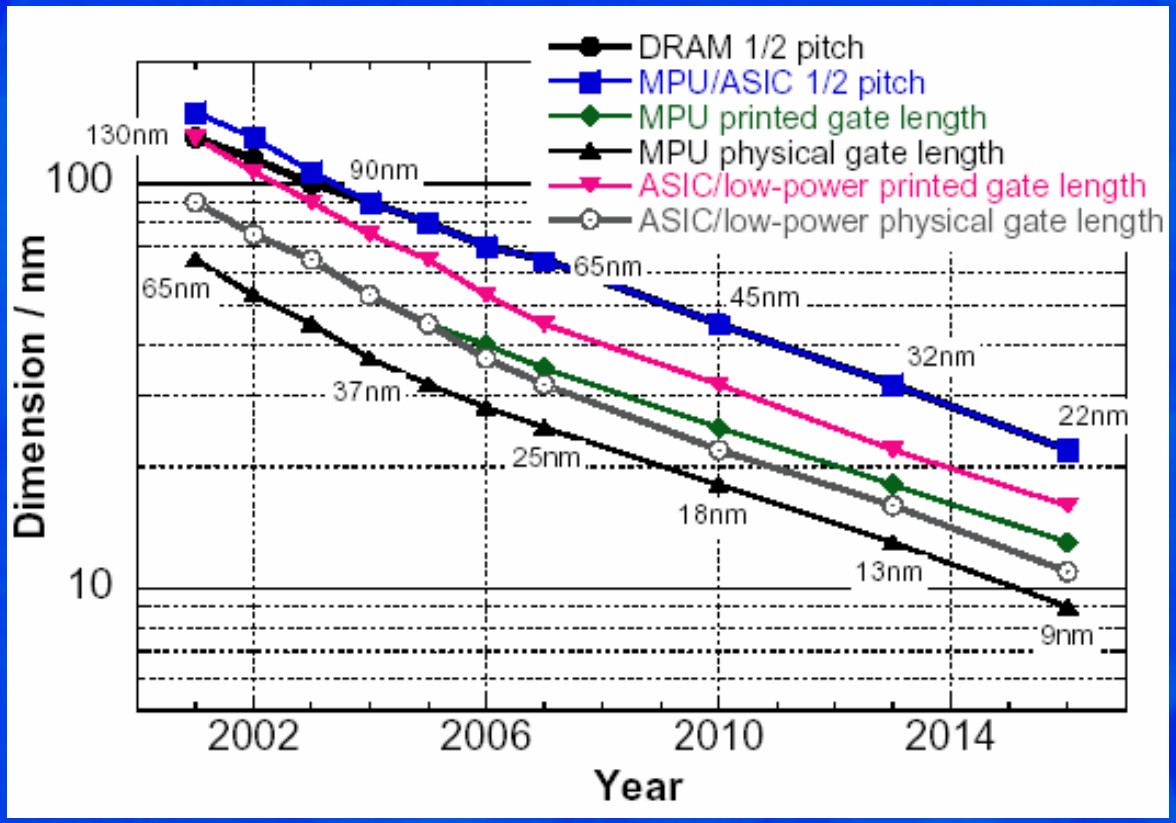
Technology nodes (1/2 pitch):

0.7 0.7

250 -> 180 -> 130 -> 90 -> 65 -> 45 -> 32 -> 22 -> 16

0.5

CMOS technology scaling



This roadmap is 5 years old:
Now 45 nm is announced in production in fall 2007 !!!

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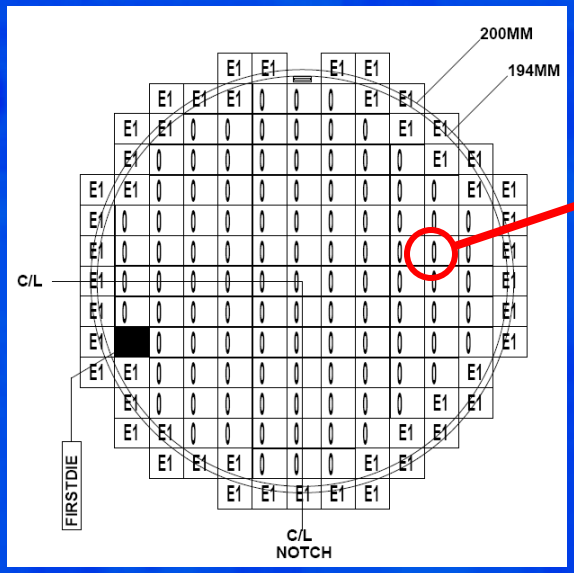
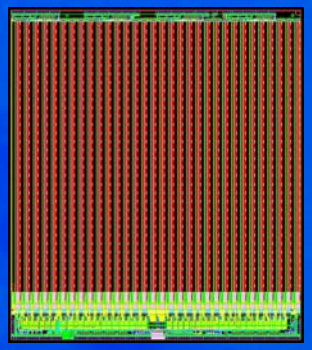
What's in a fully processed wafer?

- ✓ The repetition of a circuit (or a group of smaller circuits assembled in a "reticle") as many times as possible

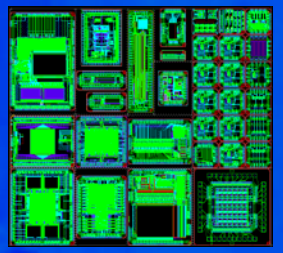
200mm wafer in its "wafer shipper" box, in the 250nm CMOS technology used for LHC



"Step plan", or map of the same wafer in the left picture. Each square is a repetition of the base structure (reticle)



Individual chip repeated in the wafer (or it could be a composition of circuits as in the figure below)



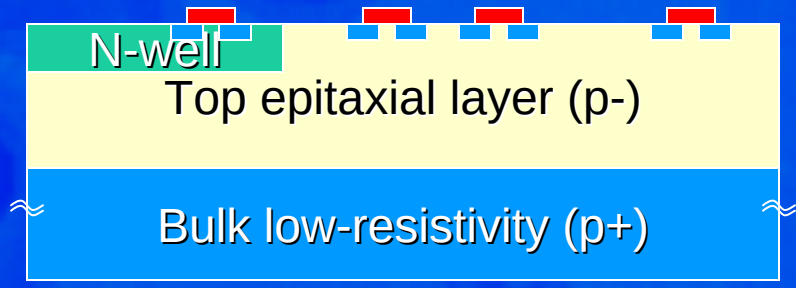
Fundamental manufacturing operations

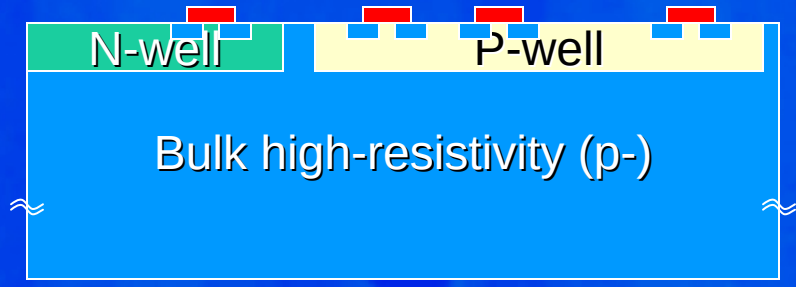
- ✓ Silicon wafer production
- ✓ Wafer cleaning
- ✓ Oxidation
- ✓ Lithography
- ✓ Ion implantation
- ✓ Etching
- ✓ Deposition

Silicon wafer production

- ✓ CMOS Foundries normally purchase substrates (silicon wafers) from other suppliers
- ✓ The wafers can be classified according to
  - Their diameter: 200mm is standard size until 130nm node, from which point also 300mm start to appear. 300mm is becoming the only option for more advanced technologies
  - Their nature: bulk, epitaxial, Silicon On Insulator (SOI)
- ✓ The native thickness of wafers is about 700μm (for 200mm), and they can be thinned after full processing with a process called Back Side Grind (BSG)

Epitaxial: bulk wafer is very low resistivity, top 2-5um are grown and have higher resistivity. Wells and diffusions are implanted on the top layer. For instance, 250nm was typically using this type of wafers.

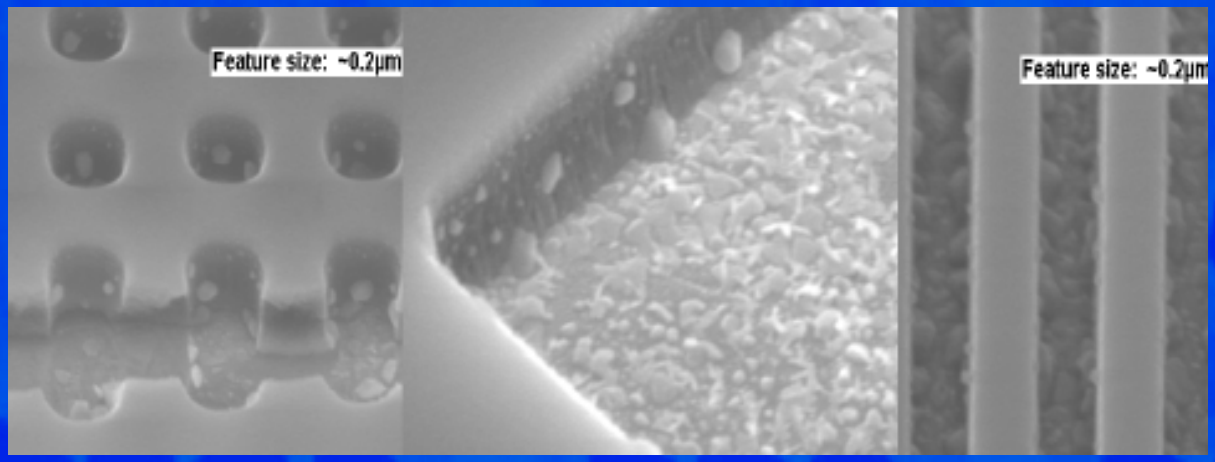




Bulk: all the wafer has rather high resistivity, and twin wells are implanted (n and p wells) on the surface with appropriate dopings for FETs. From about the 130nm node, this type of substrate is used (it is cheaper)

Wafer cleaning

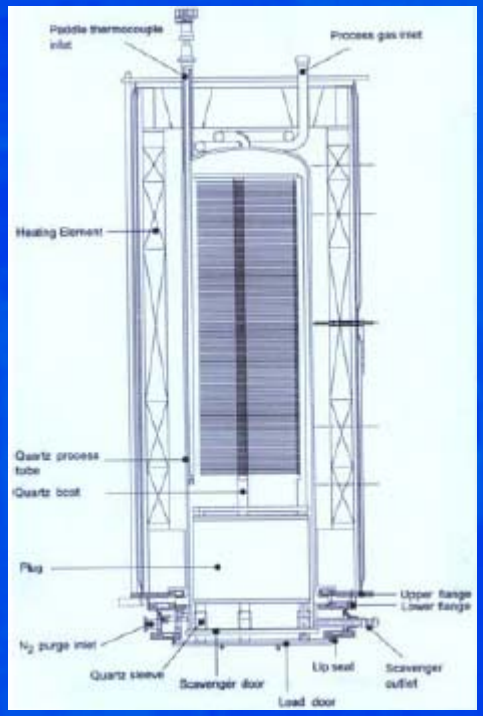
- ✓ Contamination has very strong influence on important technology properties (gate oxide integrity, poly thickness, etc.)
- ✓ Before every processing step, there is the need to removing residual contaminants from previous processing. In modern semiconductor processing, there are about 100 cleaning steps!!
- ✓ Principles of cleaning:
  - Weakening the Vad Der Waals forces sticking the contaminants to the wafer
  - Building repulsion potential around the contaminant particles and the wafer
  - Carrying away the repulsed contaminant particles from the surfaces (for instance, with physical removal mechanism such as brushing, megasonic agitation of liquids, flux of aerosols, etc.)



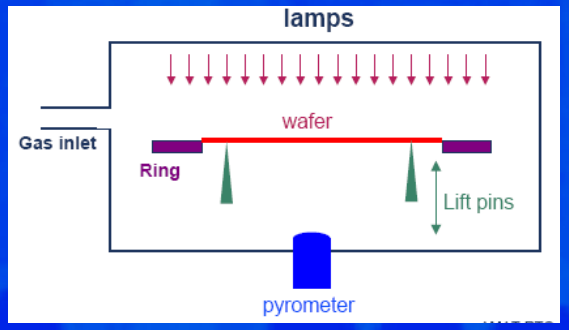
Example:
Residual polymers after etch during low-K dielectric processing. They are visible as “bubbles” in the picture and need to be removed before further processing.

Oxidation

- ✓ CMOS technologies are based on the combination of Si and SiO_2 (so far…): it is not surprising oxidation plays a fundamental role in manufacturing
- ✓ Oxide is used for the FET gate, to isolate devices from each other, to isolate metals from each other, to isolate metals from FETs
- ✓ Not all oxides are “built” with oxidation, some are deposited…
- ✓ High-quality oxides, such as the gate oxide, are product of very well controlled oxidation process (often with dopants to modify the properties of the oxide)
- ✓ Oxidation can be performed:
  - In furnaces, mainly vertical, at the batch level (more than 100 wafers at the same time)
  - In Rapid Thermal Processing (RTP) Furnaces that can process only one wafer at a time



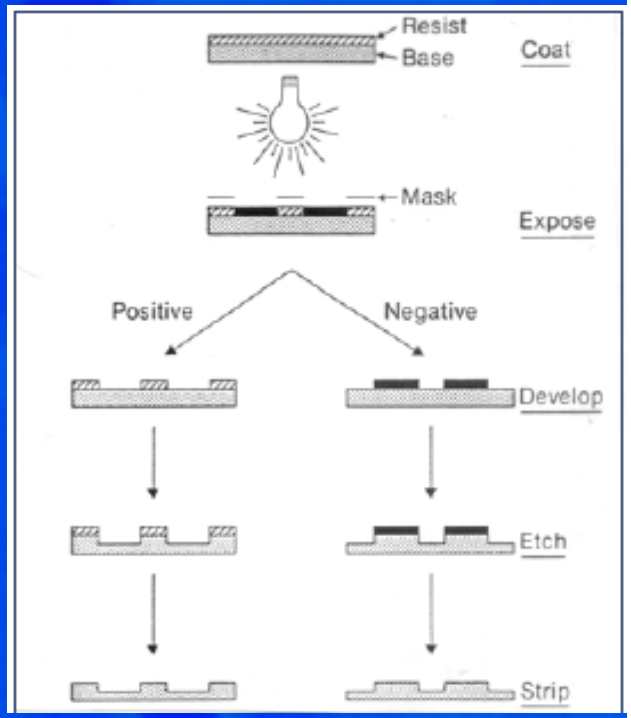
Vertical furnace for 150-175 wafers (100-150 plus dummies on top and bottom to avoid regions where T is not uniform)



RTP furnace. The wafer is heated by lamps, T is read from the back, and the wafer is rotating for better uniformity

Lithography (1)

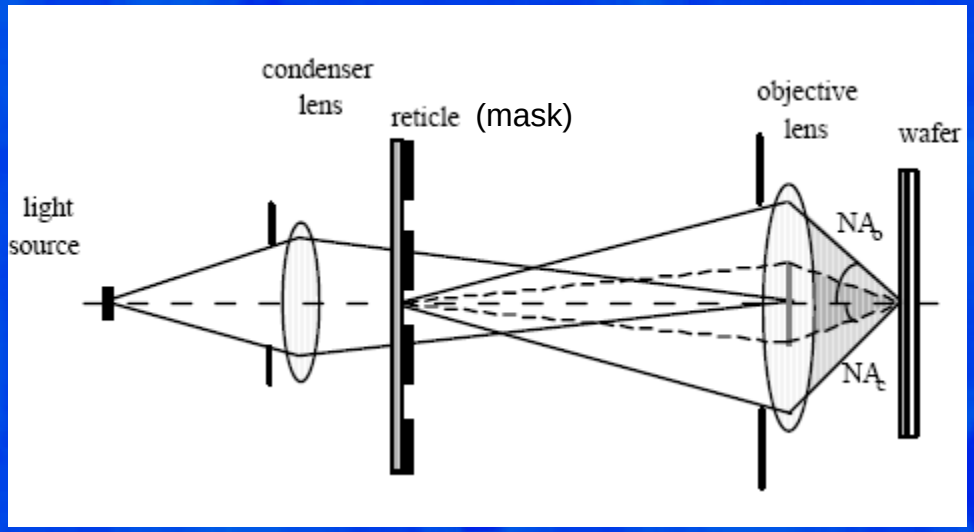
- ✓ Starting from one image of the circuit or combination of circuits (reticle), how to project this image multiple times on the wafer?
- ✓ The projection allows to "selectively" expose areas of the wafer to any given processing step (oxidation, deposition, implantation, etching, …)
- ✓ The projection field is "stepped" across the wafer regularly to reproduce the same image multiple times (actually to fill the whole wafer)
- ✓ The image to be projected – this is actually the "MASK" – is larger than its projection on the wafer, hence not too difficult to manufacture
- ✓ The process is analog to what happens in photography:
  - The wafer is covered with a material called "resist" (Coat)
  - It is then exposed to a source of light that passes through the mask. Hence the image on the mask is projected on the wafer
  - The resist changes properties only in the selected regions exposed to light
  - A "development" removes the resist only where it has changed properties (positive) or it has not changed properties (negative)
  - Now the wafer can be subject to the processing step – for instance implantation or etching – that will only take place where the resist has been removed
  - At the end, the resist will be removed from all areas and the wafer is ready for next processing step (again with selectivity determined by a new lithography step with another mask)



Example of positive or negative lithography associated with an etching step

Lithography (2)

- ✓ To improve the resolution of the image, lots of complicated “tricks” can be used:
  - On the light source (dipole, quadrupole, annular, customized, …)
  - On the mask (different types of Phase Shifting Masks, PSM)
  - With techniques such as Optical Proximity Corrections (OPC)

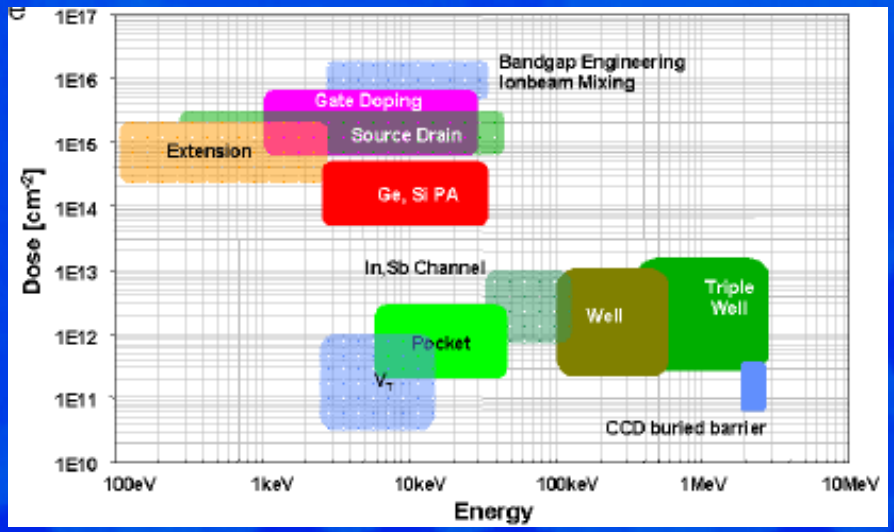


For better resolution with the same light wavelength, “immersion” lithography is used these days. The medium between the objective lense and the wafer is not air anymore, but a liquid

Light sources:
ArF (193nm) down to 65nm node
F2 (157nm wavelength) probably down to 32nm node
EUV (13.6nm wavelength) probably down to 22nm node

Ion Implantation

- ✓ Ion implantation is the standard doping technique in microelectronics
- ✓ Ions are produced in a source, mass separated in a magnet, accelerated in an electric field , deflected to obtain homogeneous doping, the implanted into the wafers
- ✓ Ion implantation produces damage which has to be annealed at high temperatures (800-1050ºC). At these elevated temperatures, dopant atoms diffuse
- ✓ The dose and energy of the ions change considerably with the purpose of the doping. Careful selection of dopant, energy, dose and annealing temperature and time allows the formation of well controlled doping profiles

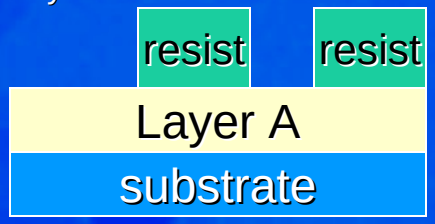


Etching

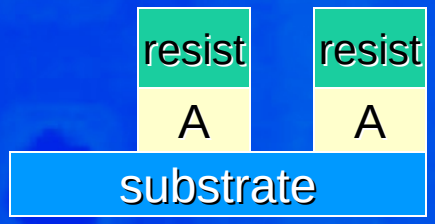
- ✓ Etching allows to removing material from the wafer surface, hence transferring a lithographic defined pattern into the underlying layer
- ✓ The most common etching technique is plasma etching, because it is:
  - Anisotropic – it enables removal of material on one direction with minimal removal on the other directions
  - Highly selective – it can be tuned to remove only one material and let the others virtually untouched
  - …and it has a large throughput, wafers can be processed quickly
- ✓ Plasma etching takes place in a chamber and in the presence of a plasma (gas mixture at low pressure with High Frequency Electric Field; this produces neutrals – atoms, radicals, molecules – ions, electrons and photons). In the plasma, the wafer surface gets quickly negatively charged and ions are accelerated towards it. Both their physical impact and – mainly – their chemistry contribute to remove material from the wafer

Example:

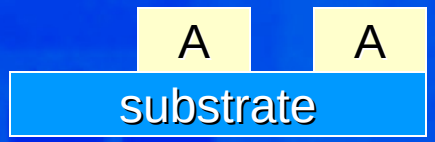
A film has to be "selectively removed" to reproduce a pattern in layer A. Lithography patterns the resist on top of the layer.



Plasma etching selectively removes layer A only, and only vertically. Etching stops when the substrate is reached (different material, or etch stop)



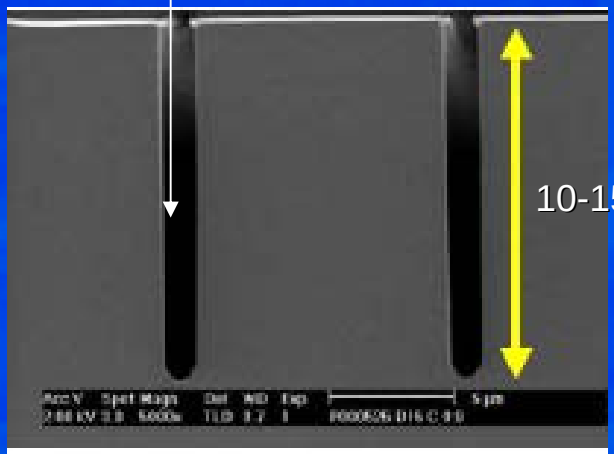
The eventual removal of the resist leaves the patterned layer A



What plasma etching can do…

Scanning Electron Microscope (SEM) images

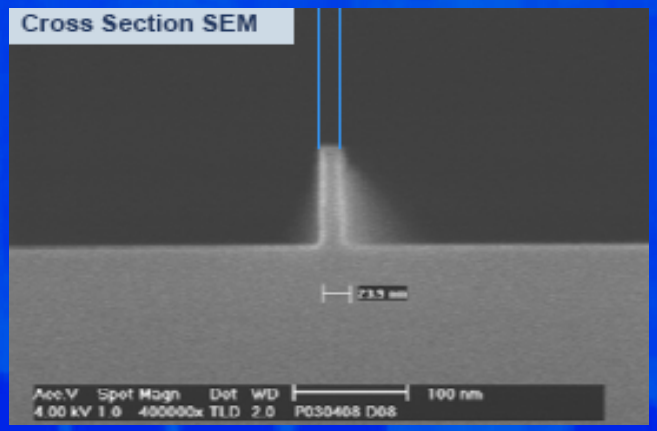
Well, this is anisotropy!

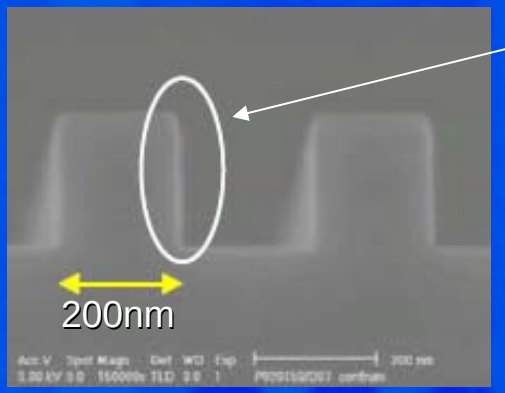


Vertical velocity of etch

$V_V = 3000$ nm/min

25nm



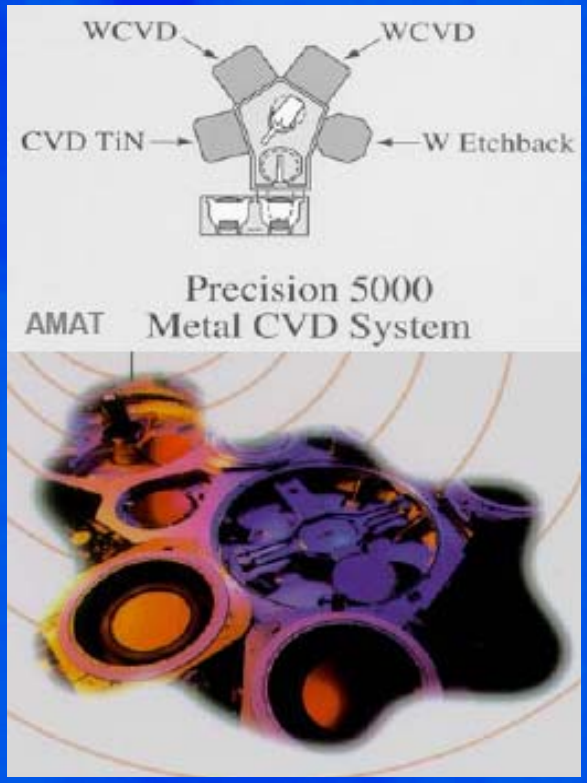


Look at the vertical profile!

Deposition

- ✓ In wafer manufacturing, one needs not only to “etch” but also to deposit material. For instance, etched holes must be filled…
- ✓ Deposition is performed with either
  - Chemical Vapor Deposition (CVD) techniques (some of which are enhanced by the presence of a plasma in the chamber). There is a large variety of such techniques: APCVD, SACVD, LPCVD, PECVD, HDPCVD, RTCVD, ALCVD…
  - Physical Vapor Deposition (PVD) techniques such as sputtering, evaporation, …
- ✓ In CVD, chemical reactions are carefully selected and enhanced by conditions in the deposition chamber (temperature, pressure, presence of plasma, …)
- ✓ Very often CVD takes place in single wafer cluster tools, where the single wafer moves from chamber to chamber to go through several processing steps

Multi-chamber tool (1 wafer per chamber at a time). In this case, the chamber does operations related to Tungsten (W) deposition for contact/via

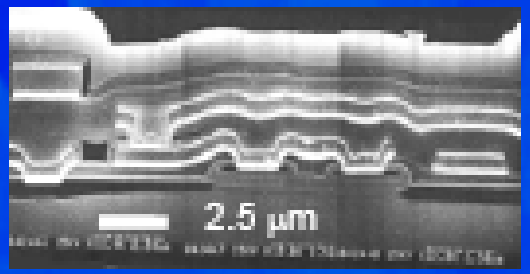


The wafer moves from one chamber to the next in sequence

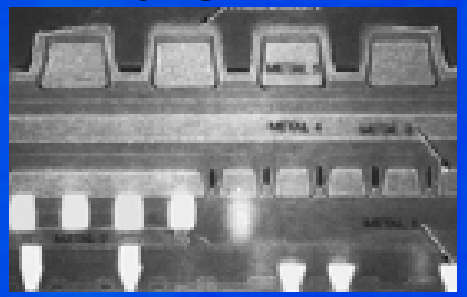
Planarization (1)

- ✓ Processing of modern technologies requires the capability of “etching” holes tens of nm wide and tens of nm apart. Up to 8 levels of metal have to be processed this way on top of each other!
- ✓ This is possible ONLY if the “substrate” is perfectly flat!
- ✓ Chemical Mechanical Polish (CMP) is the planarization process that allows modern technologies to exist
- ✓ For 90nm technology node, it allows better than 50nm planarization on a single die. This is equivalent to leveling a football field homogeneously to within better than 250μm!!!

Before CMP

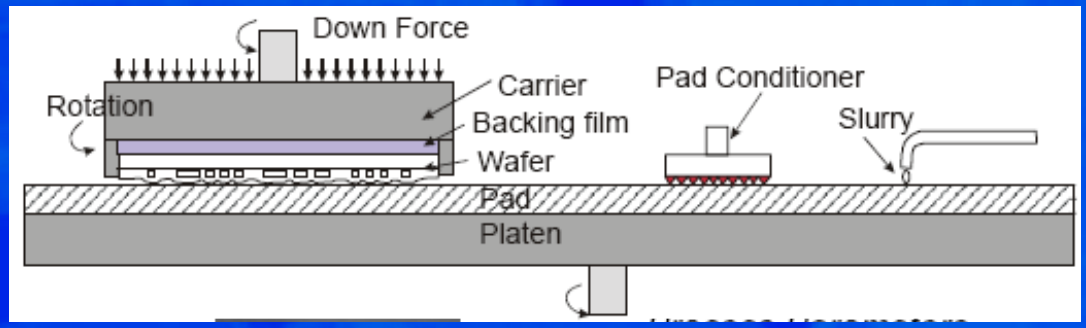


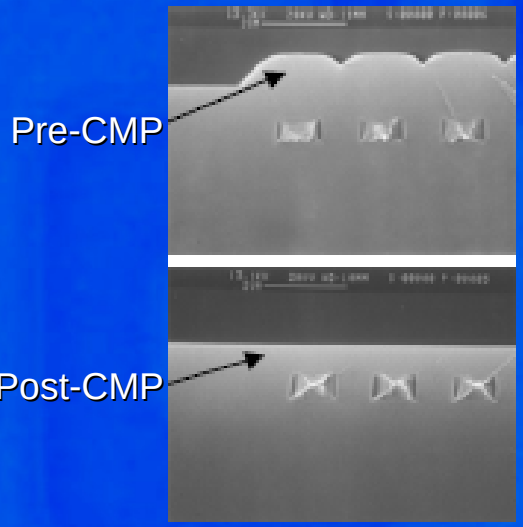
With CMP

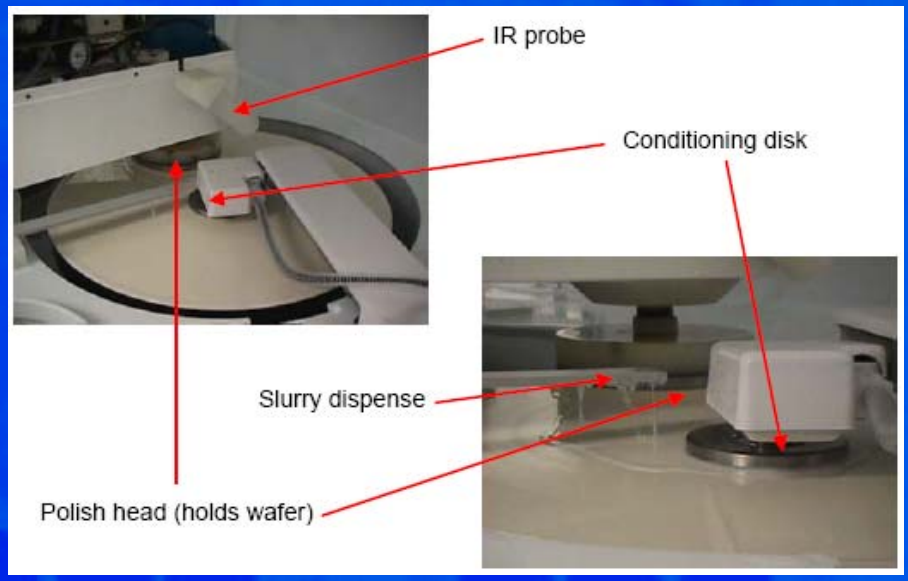


Planarization (2)

The wafer is positioned “head-down” in the CMP tool, and rotates.
The bottom platen, covered by the polishing (abrasive) pad, rotates.
A dispenser distributes a “slurry” which has a chemical action adding to the mechanical polishing.
The pad is constantly conditioned.







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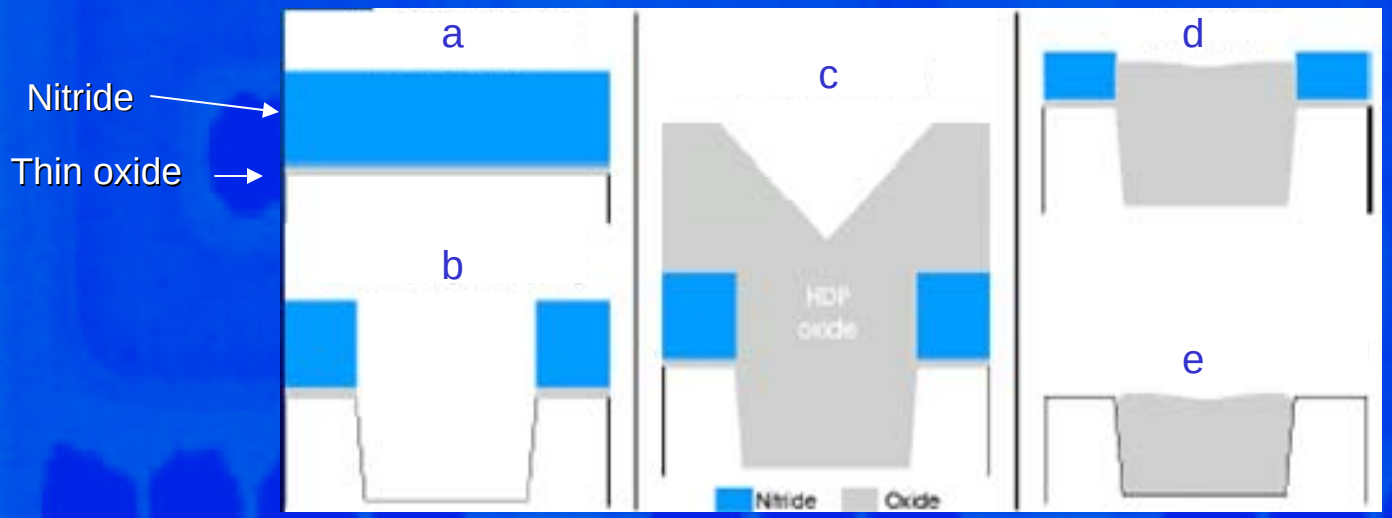
    - Front End Of Line (FEOL): construction of the transistors. The FEOL stops before the Pre-Metal Dielectric
    - Back End Of Line (BEOL)

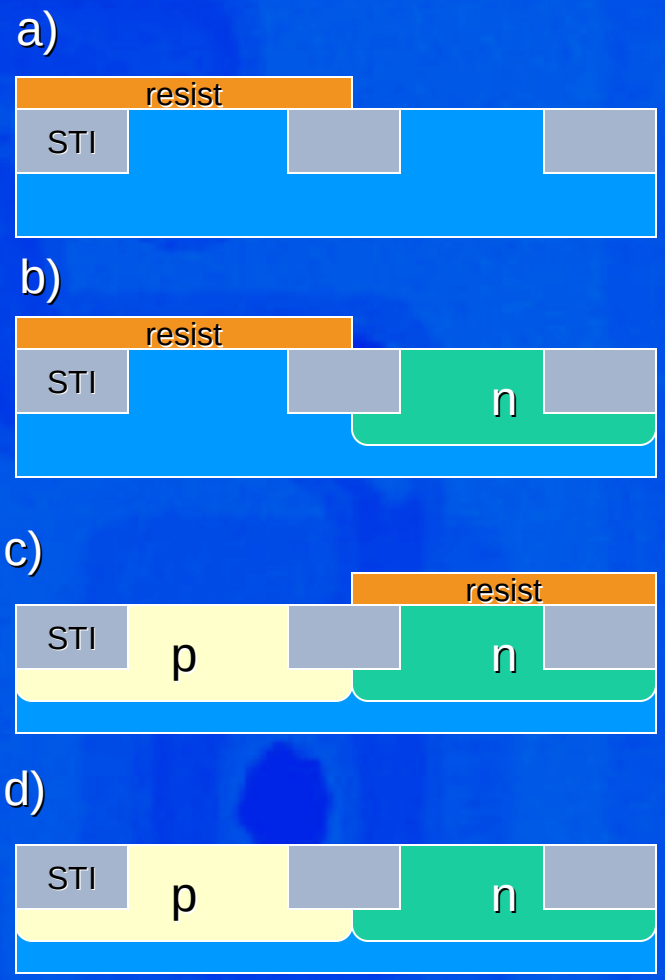
Active Area Module

- ✓ AIM: selection of “active area” (area where transistors will be built)
  - a) Thin oxide growth (thermal). Nitride (Si_3N_4) deposition
  - b) Active area patterning (lithography). Trench etching (STI trench that will isolate devices)
  - c) STI oxidation: thermal at first (thin oxide), then with High Density Plasma (HDP) CVD
  - d) Oxide planarization (CMP). Nitride is used as CMP stop point since CMP rate is much smaller in nitride than in oxide
  - e) Final result after CMP



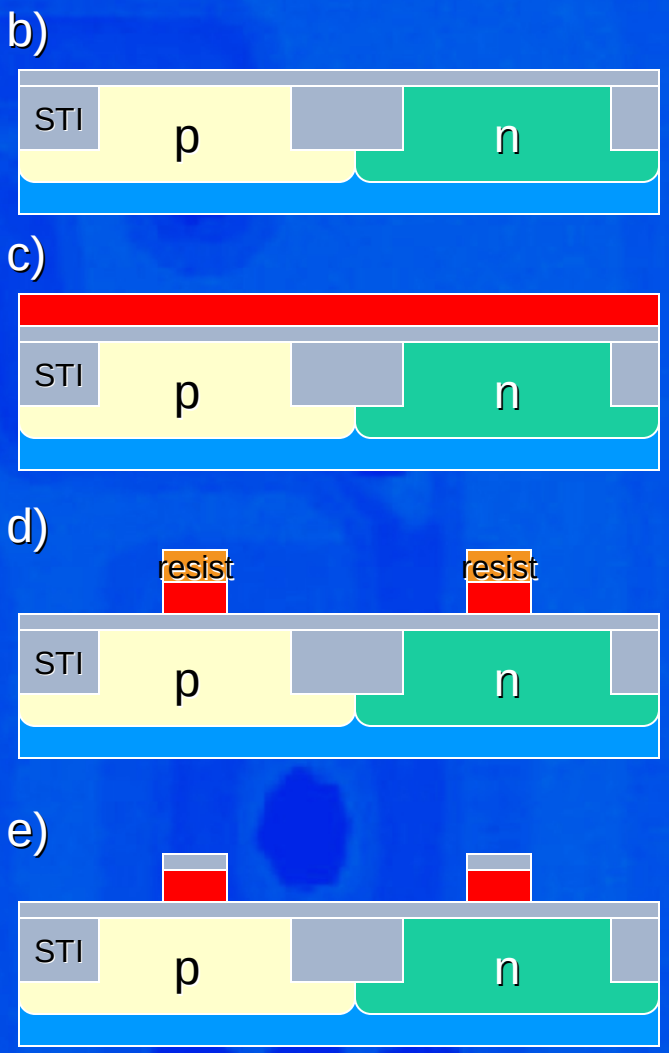
Channel doping module

- ✓ Aim: doping of the wells and doping for the threshold adjust (doping in the area where transistors will be built to fine-tune their Vth)
  - a) Definition of nwell (resist, lithograpy)
  - b) Implant of nwell in two steps: deep implant for well profile (high energy ions), shallow implant for Vth adjust and lateral leakage control
  - c) Strip resist patterning nwell, and repeat a) and b) for pwell
  - d) Well anneal (thermal process where implanted ions will diffuse)



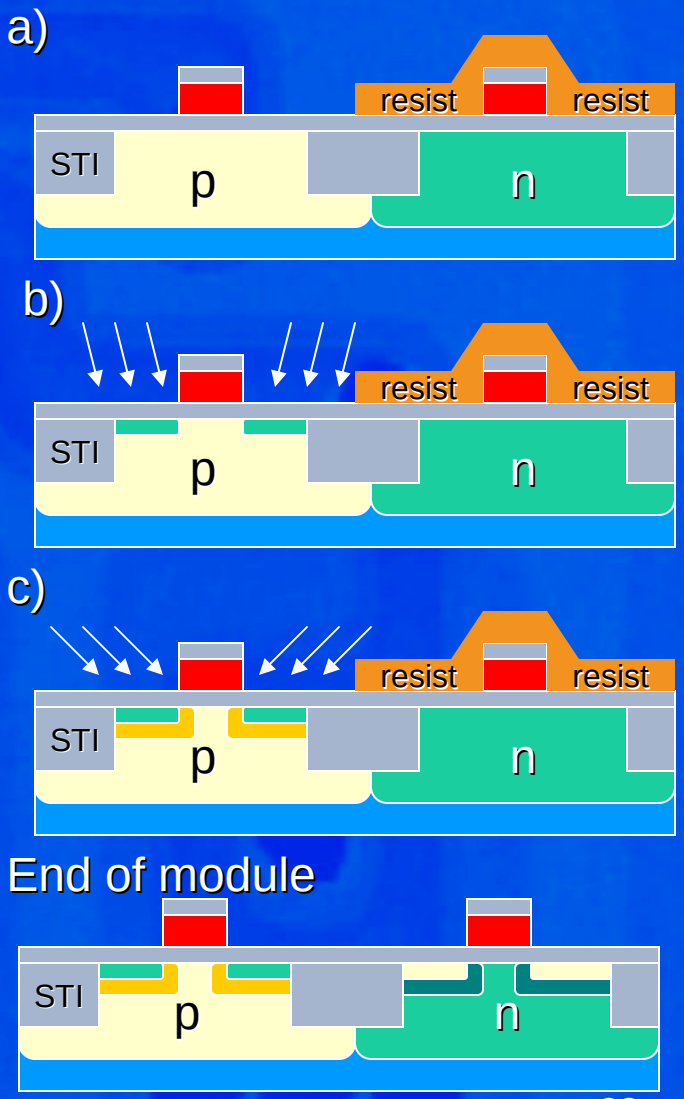
Gate module

- Aim: growing the gate oxide, deposit and pattern the polysilicon gate
  - a) Remove damaged oxide on top of active area
  - b) Gate oxide growth (nitrided oxide)
  - c) Deposition of polysilicon with CVD
  - d) Gate patterning (resist, lithography, etch)
  - e) Resist removeal (strip). Re-oxidation to cure oxide above Source/Drain areas



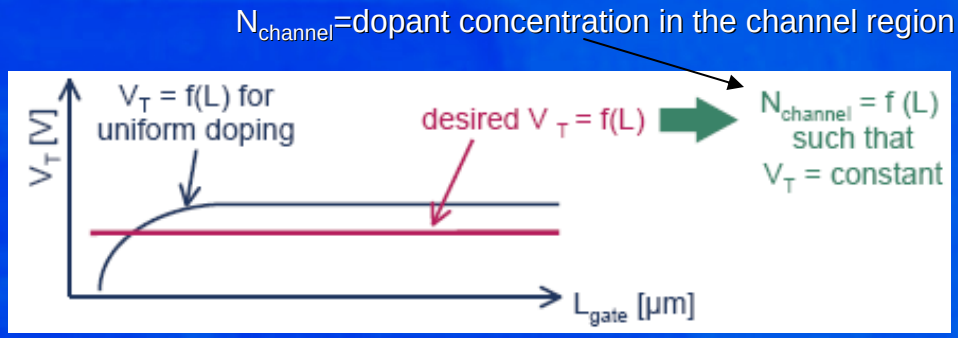
Source/Drain extension module

- ✓ Aim: implant the S/D extension and pockets (halo). The two implant are self-aligned by the presence of the poly gate
  - a) Patterning for n+ S/D (resist, lithography)
  - b) Implant of n- for S/D extension, at moderate angle (7 degrees). The extension limits the short channel effect and series R between S/D and the channel region
  - c) Implant of p- for halo, at large angle. The halo changes the channel doping concentration for short channel transistors, hence the Vth dependence on gate length is weakened
  - d) Removal of resist, RTP anneal
  - e) Repeat a) to d) for p+ S/D (all dopings are reversed)



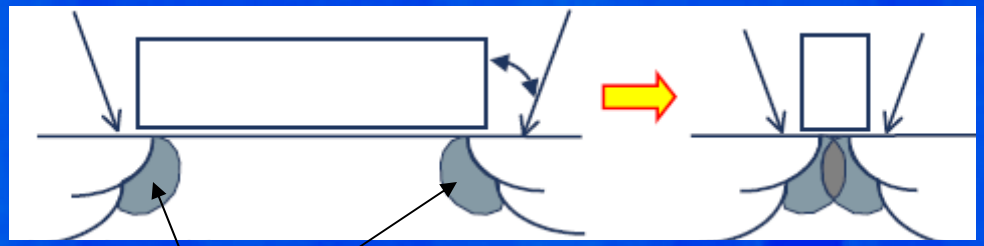
Role of the HALO implant

With uniform doping for all gate length L, Vth changes with L (Short Channel Effects). Users wish all FETs with roughly the same Vth irrespective of the L. To achieve that, HALO allows to change doping with L, so that Vth stays approximately constant



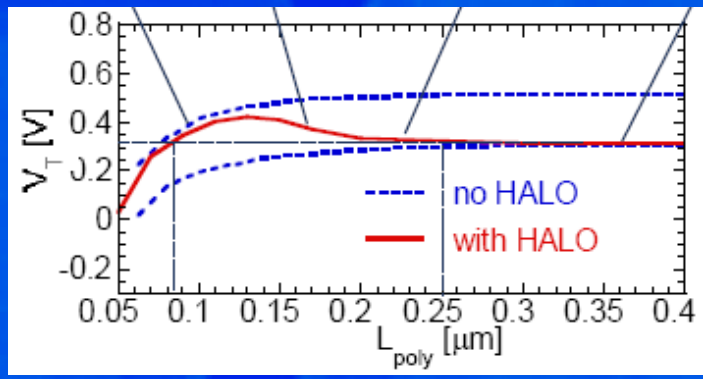
Long channel

Short channel



Halo implant

Here the doping in the channel region is higher, hence Vth is increased



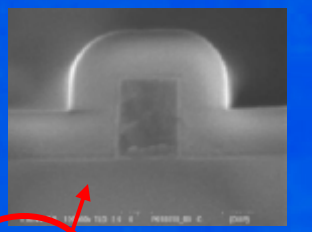
Result:

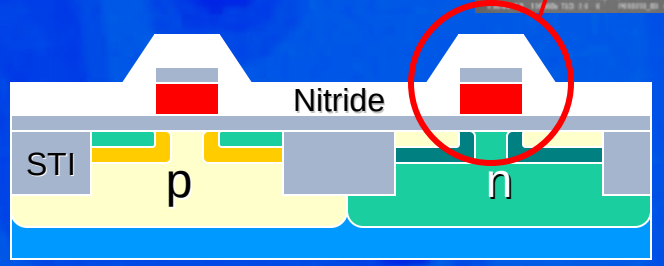
In the absence of HALO, Vth is either too low for small L or too high for large L. With HALO, the compromise is acceptable

Spacer module

- ✓ Aim: building the spacer that will allow for self-aligned S/D doping implant
  - a) Deposition of a thin oxide layer, then a thicker (150nm) nitride layer (both with CVD)
  - b) Anisotropic etching of the nitride – much quicker in vertical than horizontal direction

a)





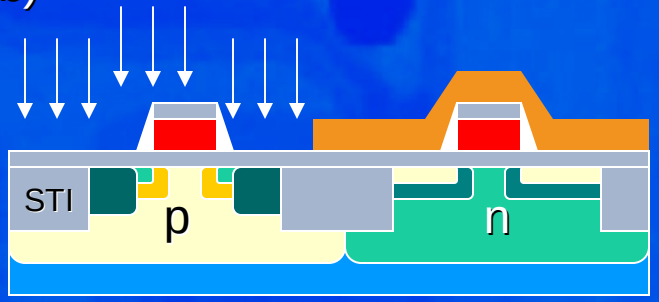
b)

Junctions module

- ✓ Aim: realizing S/D regions for FETs and doping gate electrodes
  - a) Patterning for n+ implant (NFETs)(resist, lithography)
  - b) Implant n+ regions (poly is doped as well)
  - c) Remove resist and repeat a) and b) for p+ implant (PFETs)
  - d) Remove resist. Thermal anneal to cure doping-related damage

a)

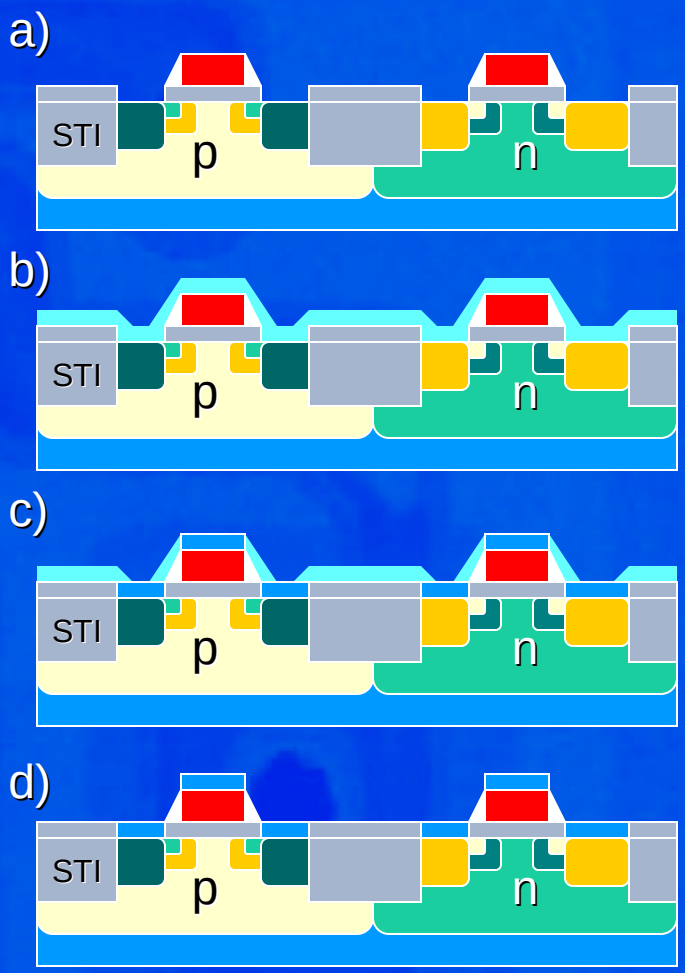
b)



End of module

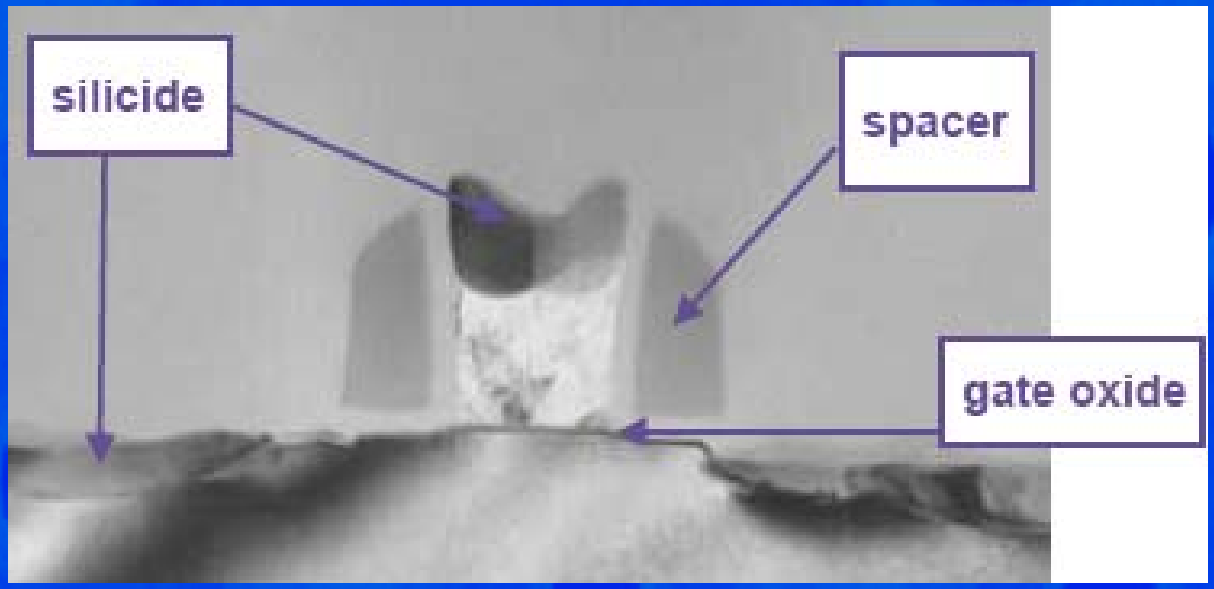
Silicide module

- ✓ Aim: Forming a silicide layer (typically $TiSi_2$ or $CoSi_2$, NiSi from the 90nm node) on top of S/D and poly to lower the access resistance
  - a) Etch of the oxide covering the Si
  - b) PVD of the metal (Ti or Co)
  - c) First RTP at lower T (order of 500°C) to form a high-resistivity compound (TiSi or CoSi). Reaction only occurs where metal is on top of silicon. Thanks to the spacers, low risk of short between S/D and poly
  - d) Etch of the metal that has not reacted with Si (selective etch)
  - e) Second RTP at higher T (order of 800°C) to continue reaction and obtain low-R compound ($TiSi_2$ or $CoSi_2$)



End of FEOL

The transistors are ready to be connected with each other and with the outer world!



SEM of a transistor at the end of FEOL

ULSI technologies: manufacturing

Outline

- ✓ Foreword
- ✓ Moore's law
- ✓ Manufacturing of ULSI CMOS technologies
  - Fundamental manufacturing operations
  - Process Flow
    - Front End Of Line (FEOL)
    - Back End Of Line (BEOL): it starts with PMD deposition. Only Copper Metal Processing flow is described here

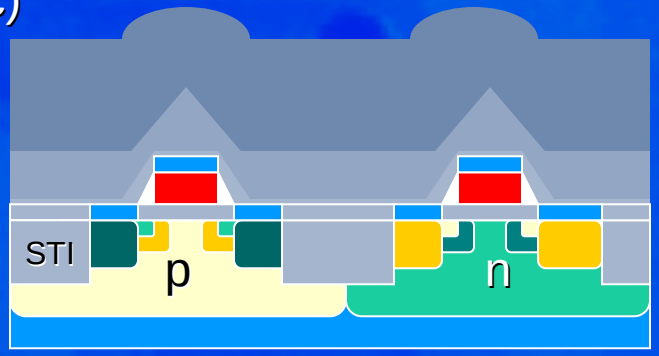
PMD module

- ✓ Aim: depositing the Pre-Metal-Dielectric insulating the silicon from the metal layers (this layer has to be a barrier against moisture and mobile ions such as K+ and Na+)
  - a) CVD of a thin layer of SiON
  - b) High Density Plasma (HDP) CVD of an Undoped Silicate Glass (USG), an SiO_2. This undoped isolation layer prevents migration of P from the upper doped layer towards Si
  - c) HDP CVD of a doped (4.5%) SiO_2 layer, PSG (Phosphosilicate Glass), that is good at capturing mobile alkali ions. This prevents migration of such ions to the Si
  - d) Anneal and CMP to about 1250nm thickness

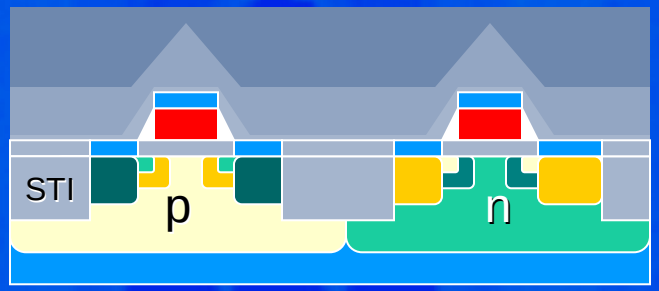
a)

b)

c)



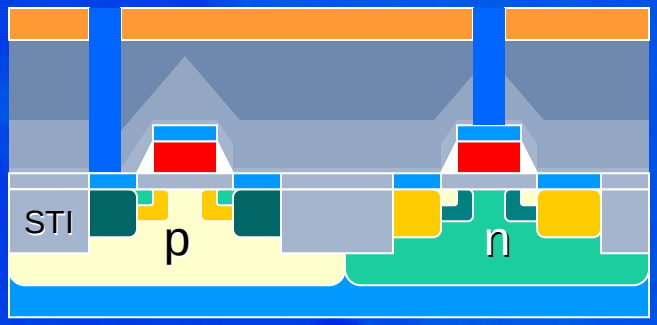
d)



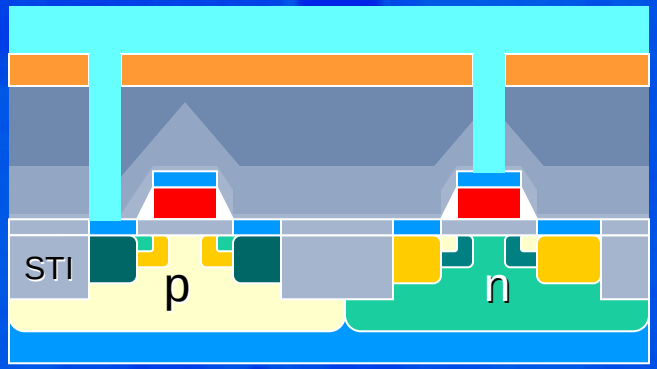
Contact module

- ✓ Aim: opening the contact holes in the PMD and filling them with tungsten (W)
  - a) Patterning for the opening (resist, lithography)
  - b) Etch of the contact hole. Etching needs to be very selective to stop on silicide (different depth of holes on poly or S/D)
  - c) Deposition (with Ionised Metal Plasma CVD) of a Ti and TiN barrier. TiN helps the following deposition of W, Ti ensures a low-R contact to the silicide. This thin layer Ti-TiN is not shown in the figures to the left, but it is present all around W in the holes
  - d) Deposition of W
  - e) CMP stopping on PSG to leave W only in the holes

b)



d)

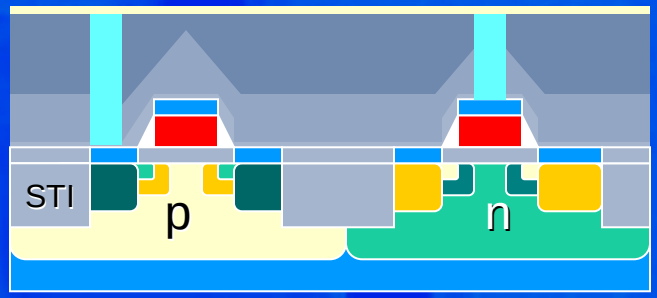


e)

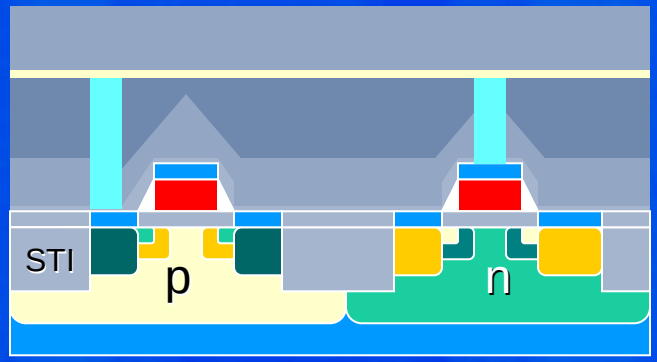
SD IMD1 module

- ✓ Aim: deposition of Inter-Metal Dielectric (IMD) in preparation of the first metal layer (metal1), that will be integrated using the Single Damascene (SD) technique
  - a) Deposition (PECVD) of a Silicon Carbide (SiC) thin layer (as etch stop material for next module, when trenches will be dug)
  - b) Deposition (PECVD) of a SiO_2 layer (IMD)

a)



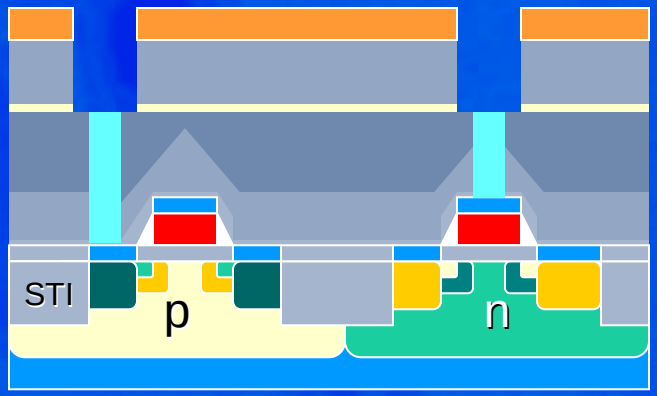
b)



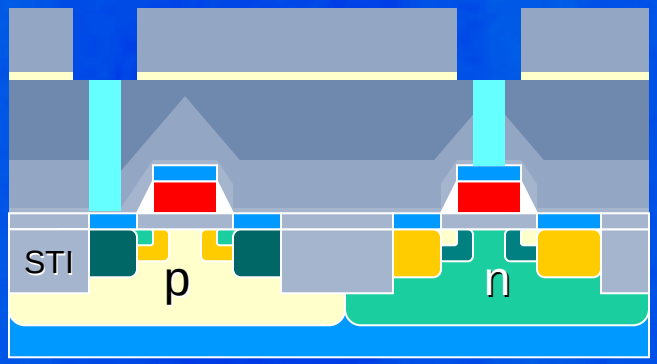
SD Metal1 patterning module

- ✓ Aim: Digging the trench for Metal1 lines
  - a) Patterning for metal1 lines (resist, lithography)
  - b) Etch of oxide and SiC
  - c) Removal of resist

a)



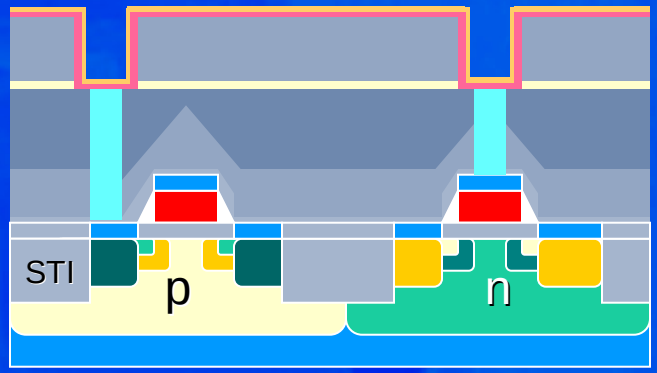
b)



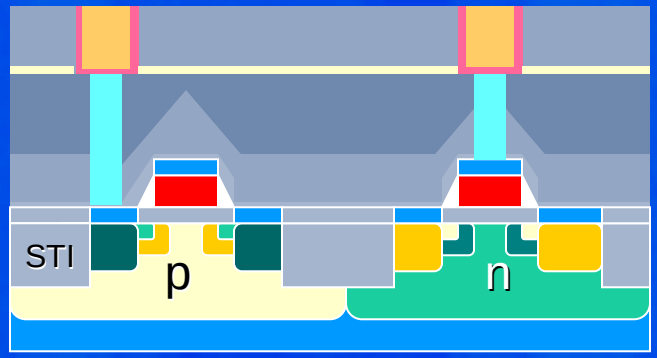
SD Cu Metal1 module

- ✓ Aim: filling the trench with Cu to complete Metal1 layer
  - a) Pre-cleaning of trench with Ar
  - b) Deposition of a TaN/Ta barrier with a PVD technique. This barrier prevents migration of Cu, since Cu has tendency to migrate
  - c) Deposition of a thin layer of Cu with the same PVD technique. This layer acts as a “seed” when later filling the trench with Cu
  - d) Deposition of the bulk of the Cu with electroplating (a form of electrolysis that takes place in a bath rich in Cu salts)
  - e) Annealing for 30” at 250°C. The annealing is necessary to ensure a change of structure of Cu, that reorganizes in larger grains with lower resistivity
  - f) CMP of the Cu, then of the TaN/Ta barrier. In this phase, it is necessary to have uniform Cu distribution across the wafer to have good results (this drives strict requirements for pattern density)

c)



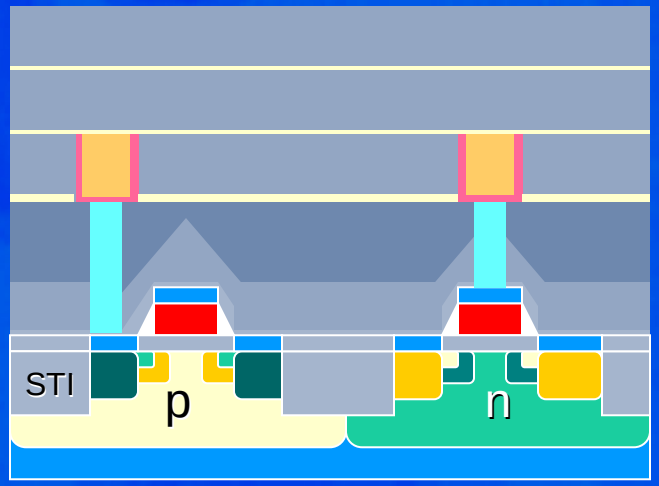
f)



DD IMD2 module

- ✓ Aim: deposition of Inter-Metal Dielectric (IMD) in preparation of the second metal layer (metal2), that will be integrated using the Double Damascene (DD) technique
  - a) Deposition (PECVD) of a Silicon Carbide (SiC) thin layer (as etch stop material for next module, when trenches will be dug)
  - b) Deposition (PECVD) of a SiO2 layer (IMD)
  - c) Steps a) and b) are repeated

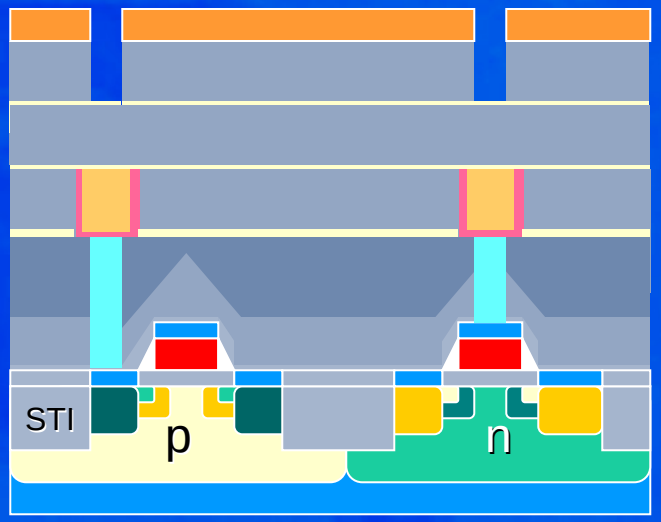
c)



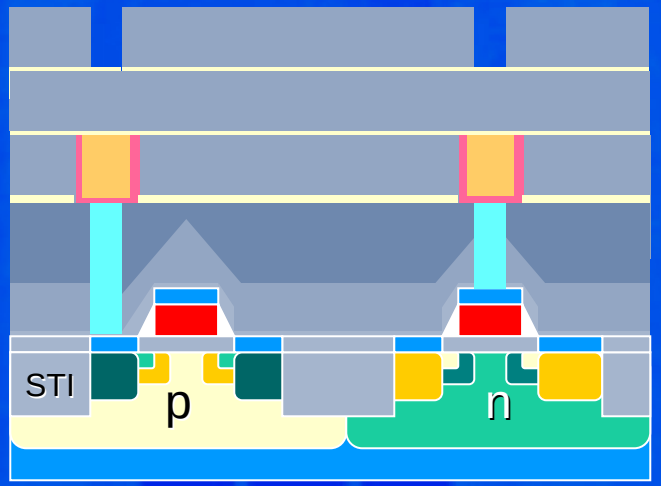
DD Metal2 patterning module (1)

- ✓ Aim: Patterning the dielectric to prepare for the deposition of Cu for M1-M2 vias and for Metal2
  - a) Patterning for Via1 holes (resist, lithography)
  - b) Partial Via1 etch, using the top SiC layer as etch stop
  - c) Removal of resist

b)



c)



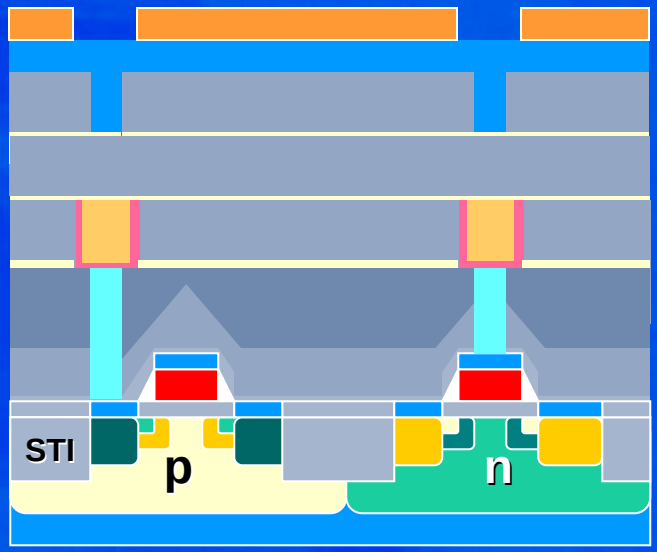
DD Metal2 patterning module (2)

d) Deposition of an “underlayer” (UL) resist (planarized)

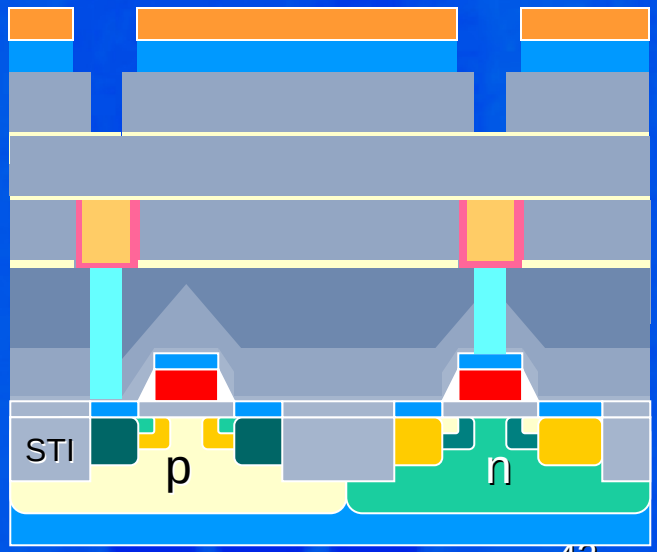
e) Deposition of an Imaging Layer (IL) of resist, and pattern of this layer for Metal1

f) Development of the UL resist in plasma, very selectively under openings of IL and until trenches are completely emptied

e)



f)

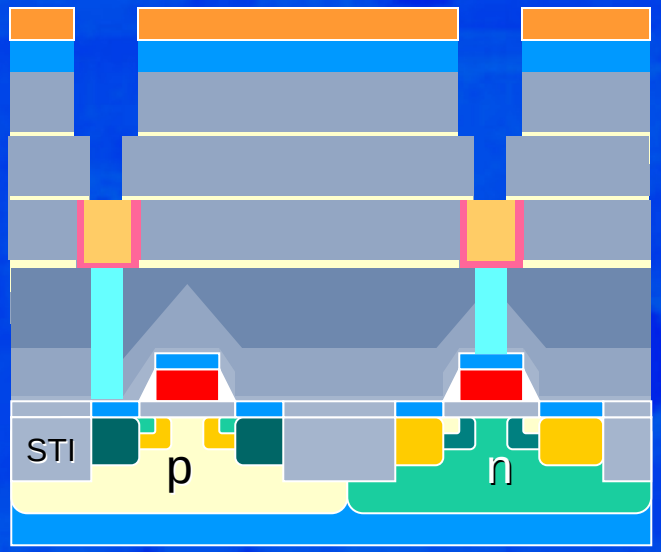


DD Metal2 patterning module (3)

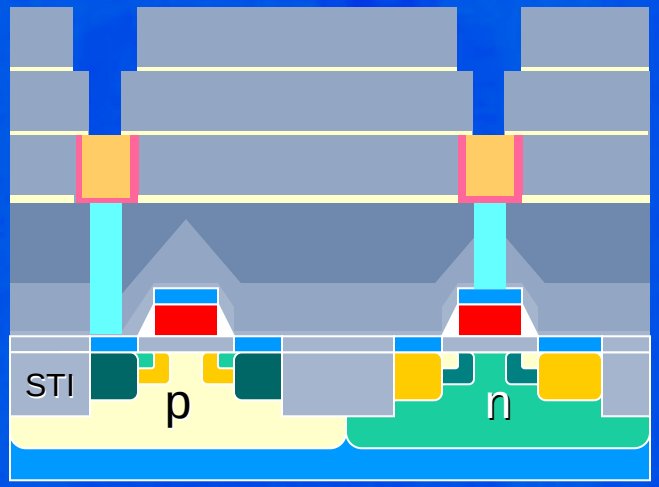
g) Damascene etch of the oxide for both Via1 and Metal2 (SiC layers as etch stop)

h) Removal of resist

g)

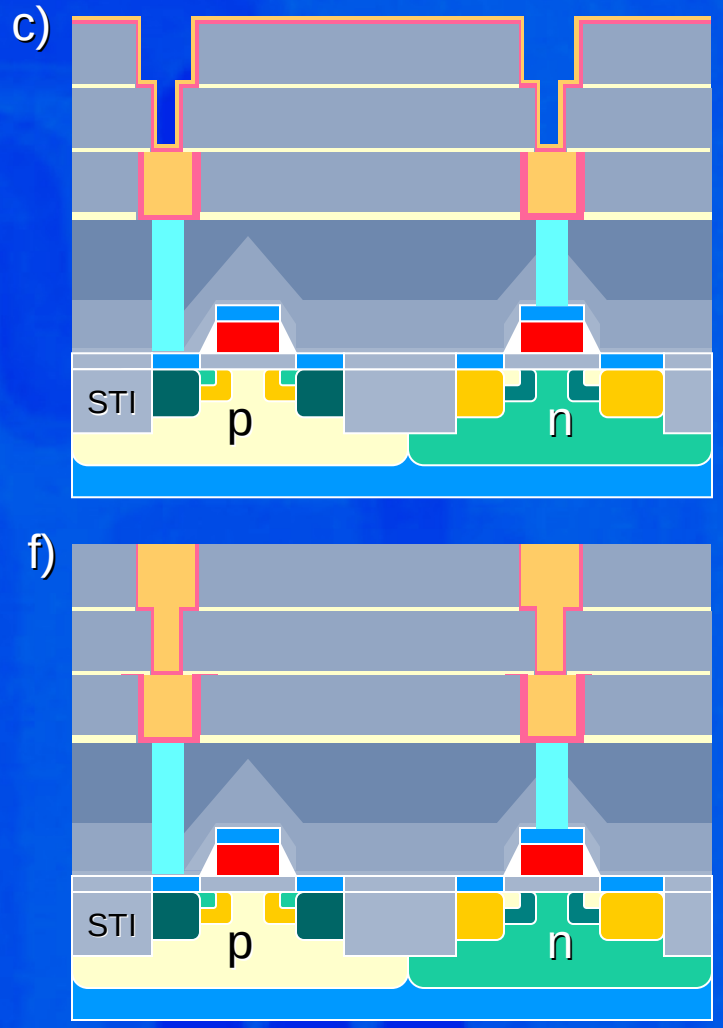


h)



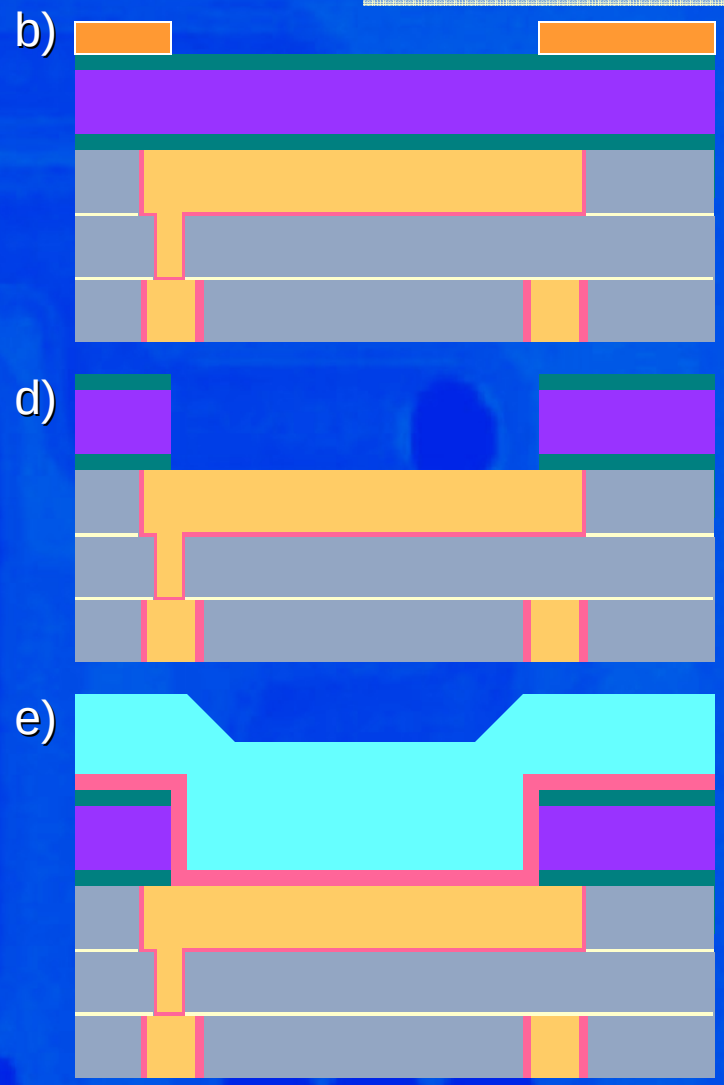
DD Cu Metal2 and Via1 module

- Aim: filling the trenches with Cu for both Via1 and Metal2. The procedure is identical to the one used already for Metal1
  - a) Pre-cleaning of trench with Ar
  - b) Deposition of a TaN/Ta barrier with a PVD technique. This barrier prevents migration of Cu, since Cu has tendency to migrate
  - c) Deposition of a thin layer of Cu with the same PVD technique. This layer acts as a "seed" when later filling the trench with Cu
  - d) Deposition of the bulk of the Cu with electroplating (a form of electrolysis that takes place in a bath rich in Cu salts)
  - e) Annealing for 30" at 250°C. The annealing is necessary to ensure a change of structure of Cu, that reorganizes in larger grains with lower resistivity
  - f) CMP of the Cu, then of the TaN/Ta barrier. In this phase, it is necessary to have uniform Cu distribution across the wafer to have good results (this drives strict requirements for pattern density)
- All other metal layers are processed the same way (Double Damascene)



Passivation module (1)

- Aim: at the end of the metal stack (up to 8 levels), the final passivation and the pad opening steps are performed
  - a) Deposition of a stack (SiC, Nitride, SiC)
  - b) Patterning of the pad opening (resist, lithography)
  - c) Etch of top SiC layer. Resist removal
  - d) Etch of Nitride and bottom SiC layer
  - e) Deposition of TaN (barrier) and Aluminum



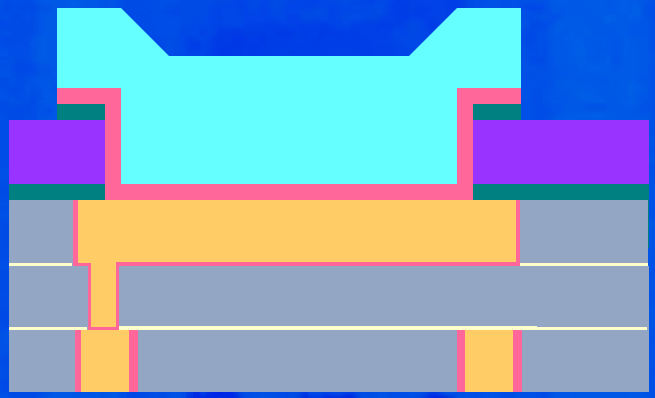
Passivation module (2)

f) Patterning of the Al pad (resist, lithography)

g) Etch of Al and TaN. Resist removal

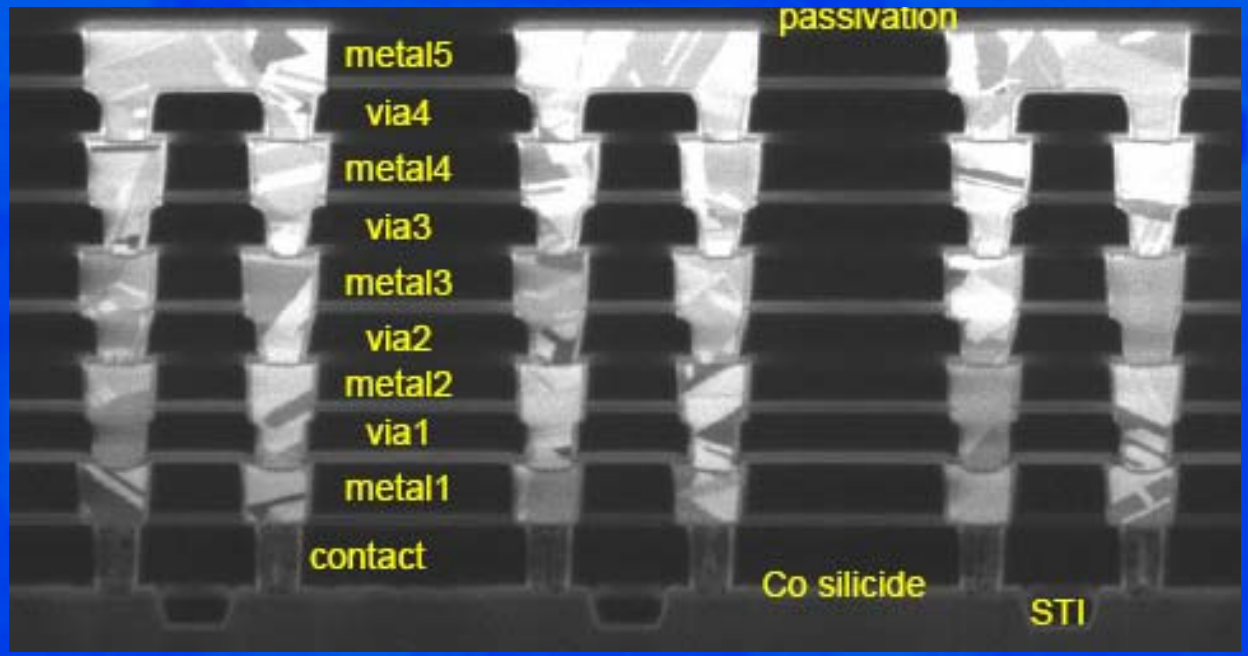
f)

g)



End of BEOL

The wafers are finished, ready for being thinned, diced and packaged



Example: 5 metal stack (all Cu)

To study further…

- ✓ M.Quirk, J.Serda, “Semiconductor Manufacturing Technology”, Prentice Hall, ISBN 0-13-081520-9
- ✓ 1-week course “Silicon Processing for ULSI circuit fabrication”, organized yearly by MTC (Microelectronics Training Center) of IMEC, know also as “Tauber course”
- ✓ To keep updated with newest technologies, attend the IEDM conference (typically in December in either Washington or San Francisco)
- ✓ On the net, to follow latest developments and news from Industry:
  - http://www.fabtech.org/
  - http://www.reed-electronics.com/semiconductor/index.asp?rid=0&rme=0&cfd=1

General Outline

- ✓ ULSI technologies: manufacturing
- ✓ Radiation effects in devices and technologies
- ✓ Radiation Hardness-By-Design (HBD) techniques for ASICs
- ✓ 130nm technology node for High Energy Physics: vendor, properties, radiation effects

Radiation effects in devices and technologies

Outline

- ✓ General view
- ✓ Total Ionizing Dose (TID)
- ✓ Displacement damage
- ✓ Single Event Effects
  - SEU, SET
  - Destructive events

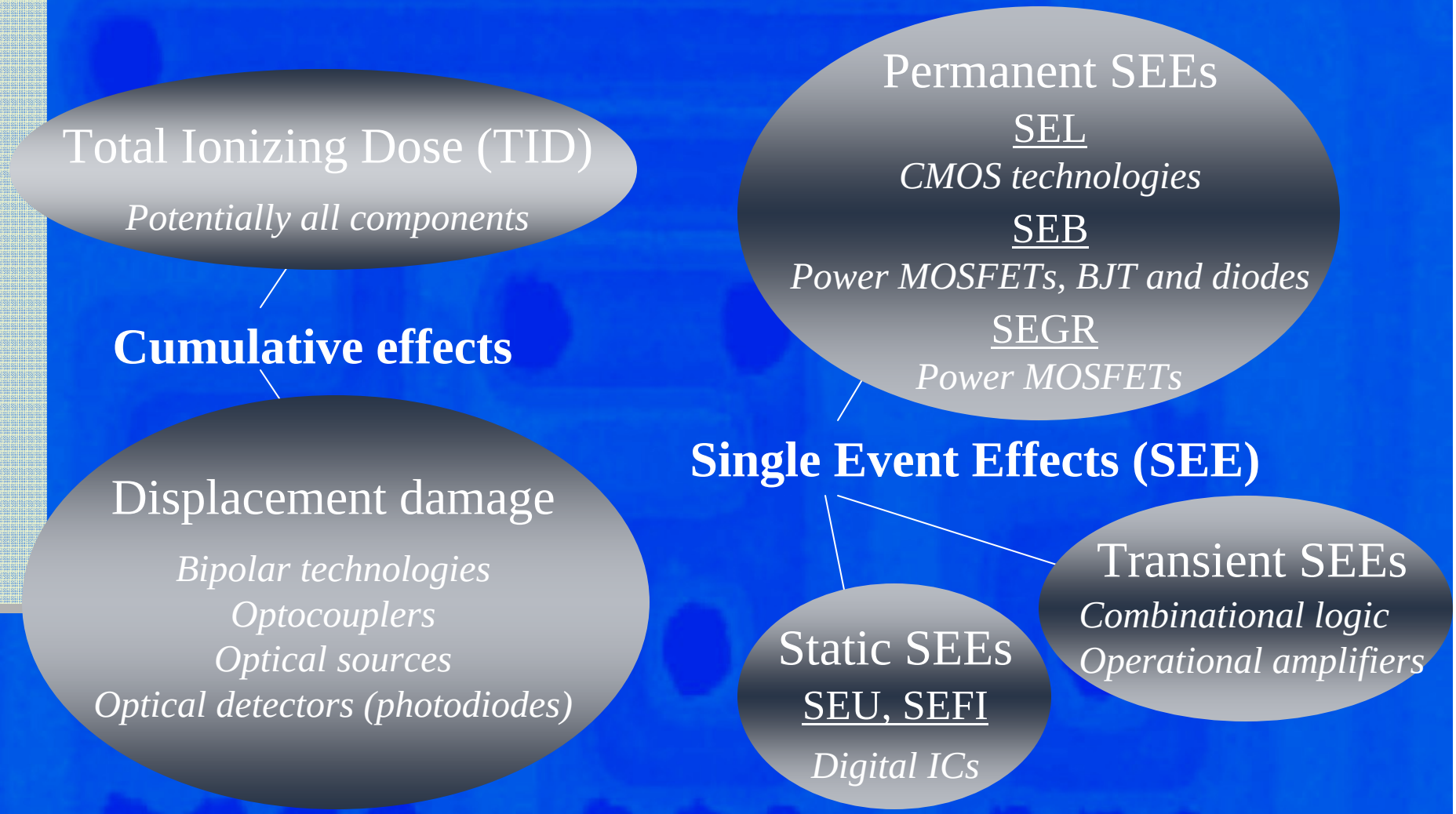
Radiation Levels in ATLAS

During the experiment lifetime (10 years)

Detector zone	Total dose [rd]	Neutrons (1 MeV eq.) [n/cm^2]	Charged hadrons (> 21 MeV) [n/cm^2]
Pixels	112 M	$1.47 \cdot 10^{15}$	$2 \cdot 10^{15}$
SCT Barrel	7.9 M	$1.4 \cdot 10^{13}$	$1.1 \cdot 10^{14}$
ECAL (barrel)	5.1 k	$1.7 \cdot 10^{12}$	$3.6 \cdot 10^{11}$
HCAL	458	$2.5 \cdot 10^{11}$	$5.6 \cdot 10^{10}$
Muon det.	24.3 k	$3.8 \cdot 10^{12}$	$8.7 \cdot 10^{11}$

- TID = energy deposited via ionization per unit mass SI unit = Gy = 100 rd
- Neutron and Ch. Hadrons “intensities: are expressed in fluence = integral of flux over time (10 years in this case)
- Hadrons are particles subject to the strong interaction, mainly p and n (and pions) in our context

Summary of radiation effects

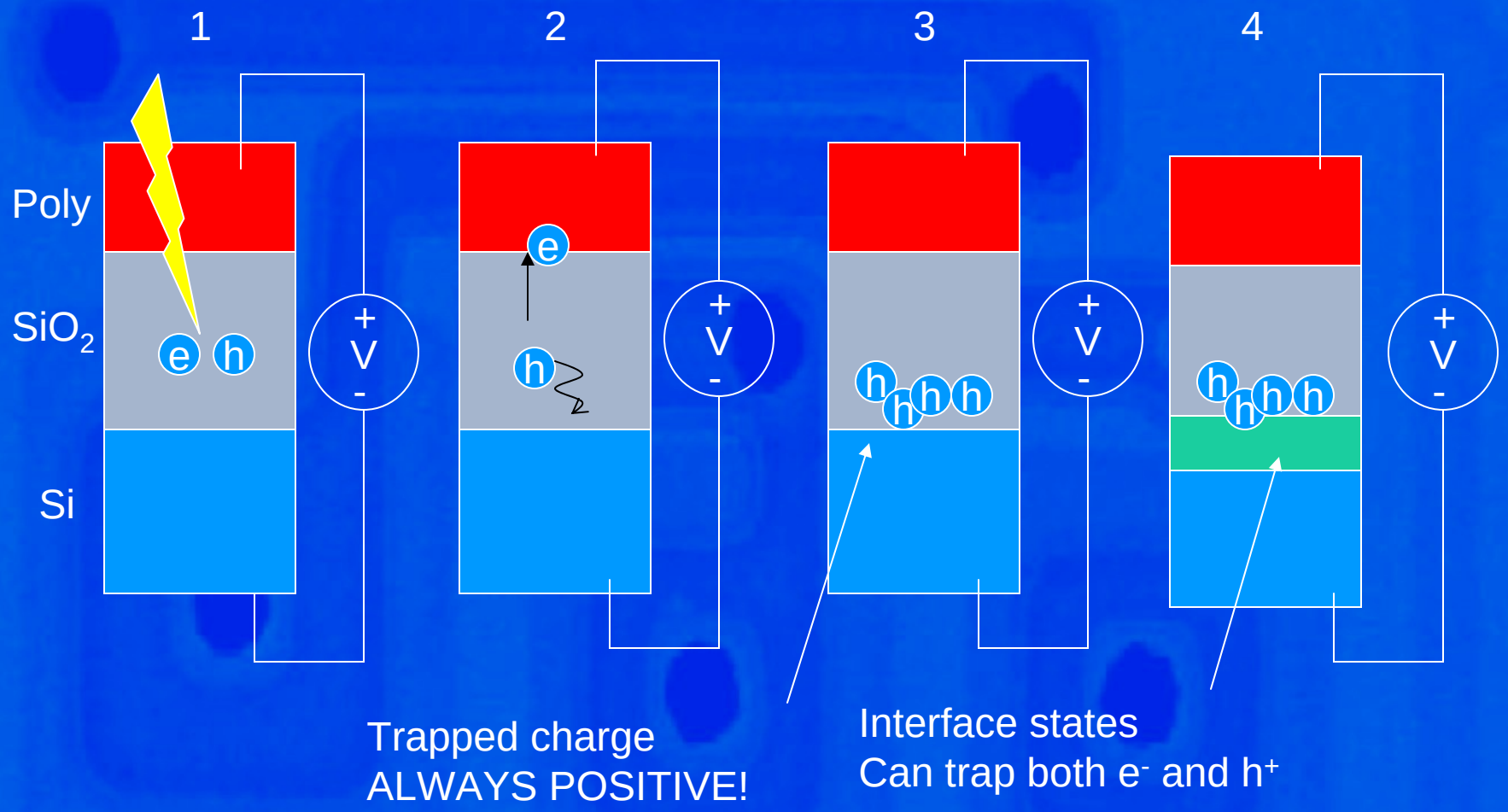


Radiation effects in devices and technologies

Outline

- ✓ General view
- ✓ Total Ionizing Dose (TID)
  - TID in CMOS technologies
  - TID in bipolar technologies
- ✓ Displacement damage
- ✓ Single Event Effects
  - SEU, SET
  - Destructive events

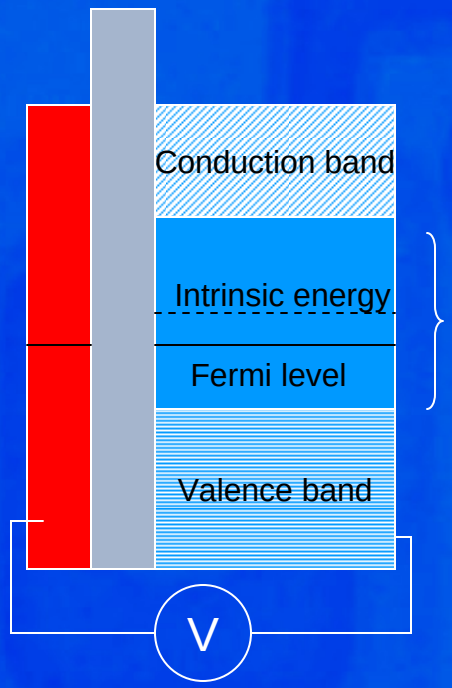
TID in MOS structures



Role of interface states

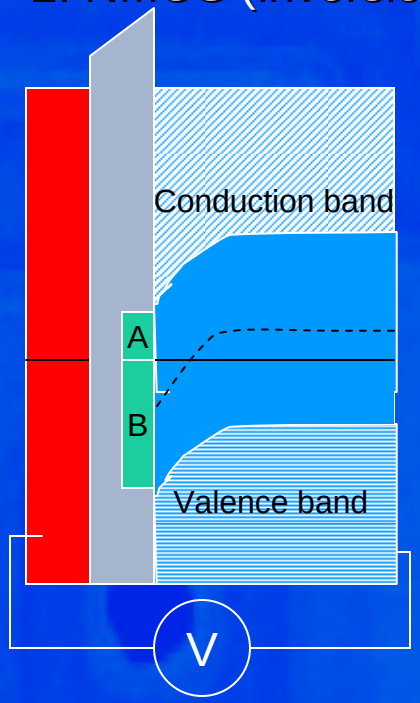
Interface states can trap charge of both polarities.
What is their role for NMOS and PMOS structures?

1. Flatband



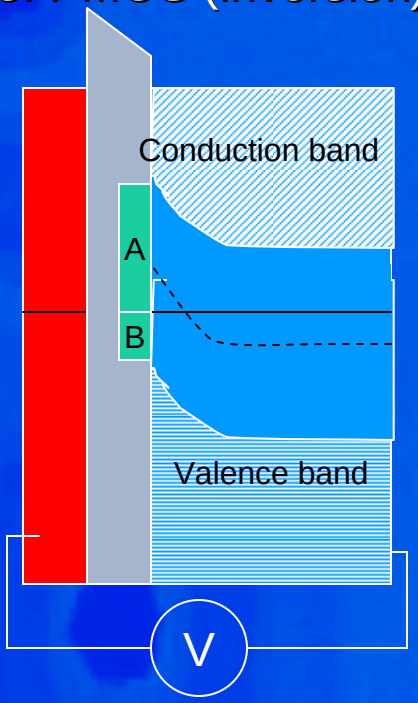
Forbidden gap

2. NMOS (inversion)



In NMOS, negative charge is trapped

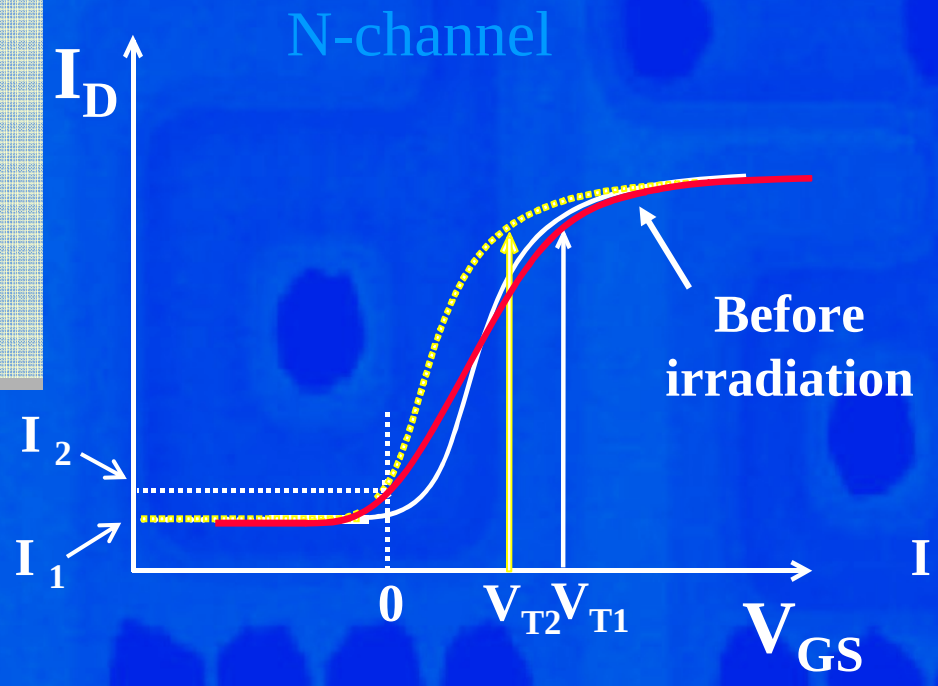
3. PMOS (inversion)

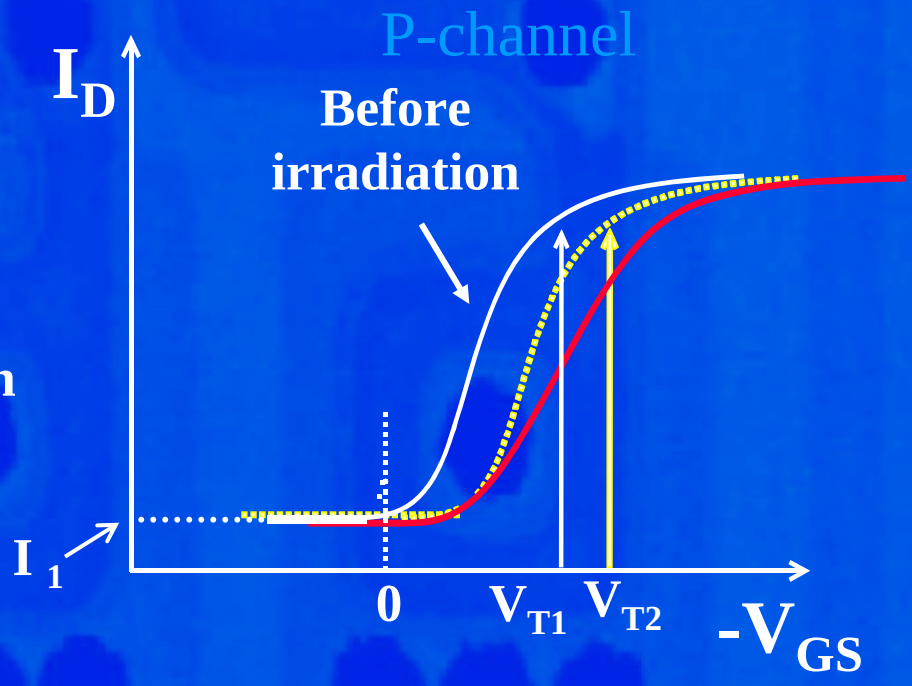


In PMOS, positive charge is trapped

Contributions to the V_T shift

	n-channel	p-channel
• Oxide charges	—	—
• Interface states	+	—

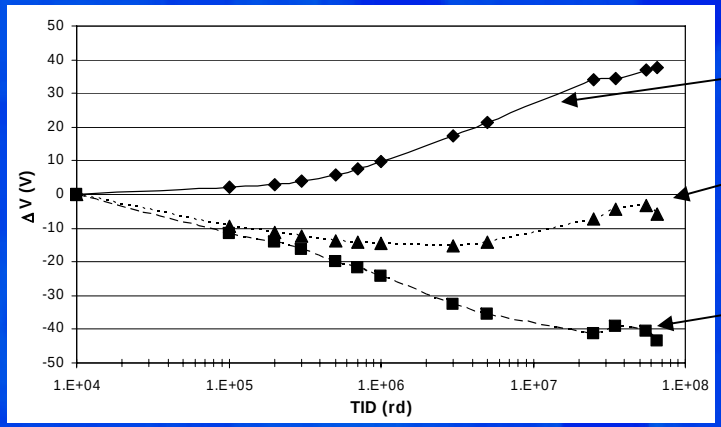




Different evolution of defects

- All charge trapped in the oxide or in the interface states affect the electric field across the oxide (hence the Vt of the structure).
- The evolution of charge trapping and interface state formation during and after irradiation is different. This is very relevant for the overall evolution of the measured behavior.

Example: very thick oxide NMOS



Contrib from interface states

Net effect on Vth

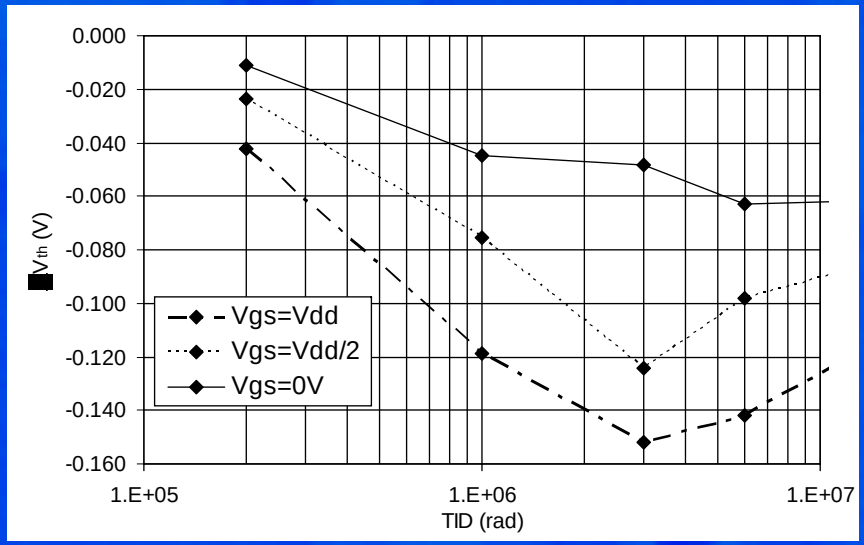
Contrib from charge trapped in oxide

- Annealing, or self-healing, is typically driven by thermal energy or hopping of carriers from the Si layer (only about 3nm range). It is normally effective for trapped charge only, not for interface states (exception recently pointed out for thick field oxides)

Bias dependence

Bias condition during irradiation is VERY relevant for the radiation effects. During irradiation, the worst-case bias condition "pushes" holes towards the Si-SiO_2 interface.

Example: Vth shift of NMOS in 3 different bias conditions

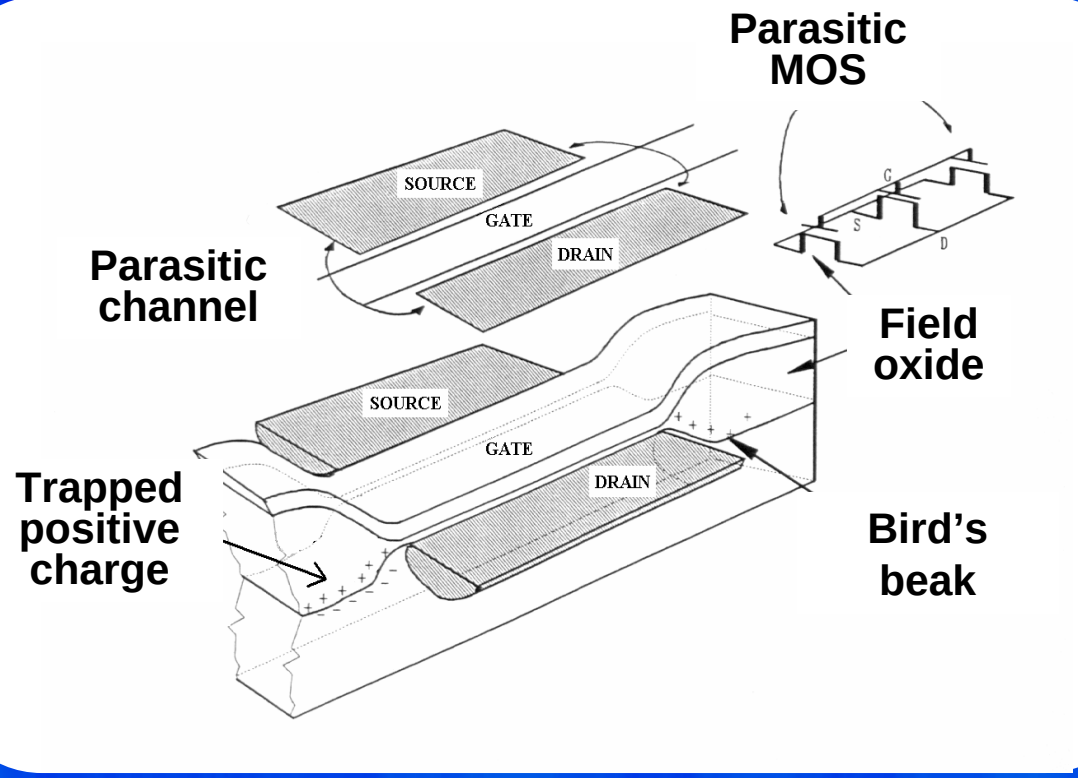


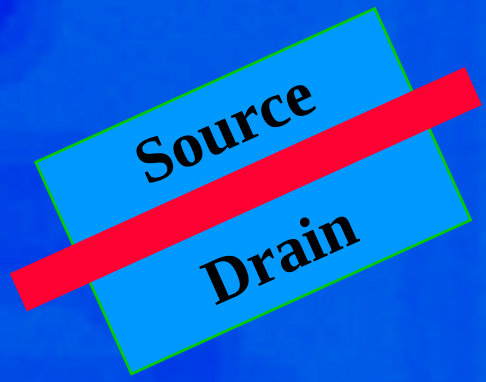
CMOS 130nm tech
W/L=0.16/0.12um

The larger the positive bias, the larger the Vth shift

RULE: Power circuits in their operational condition, or a condition known to be worst-case!

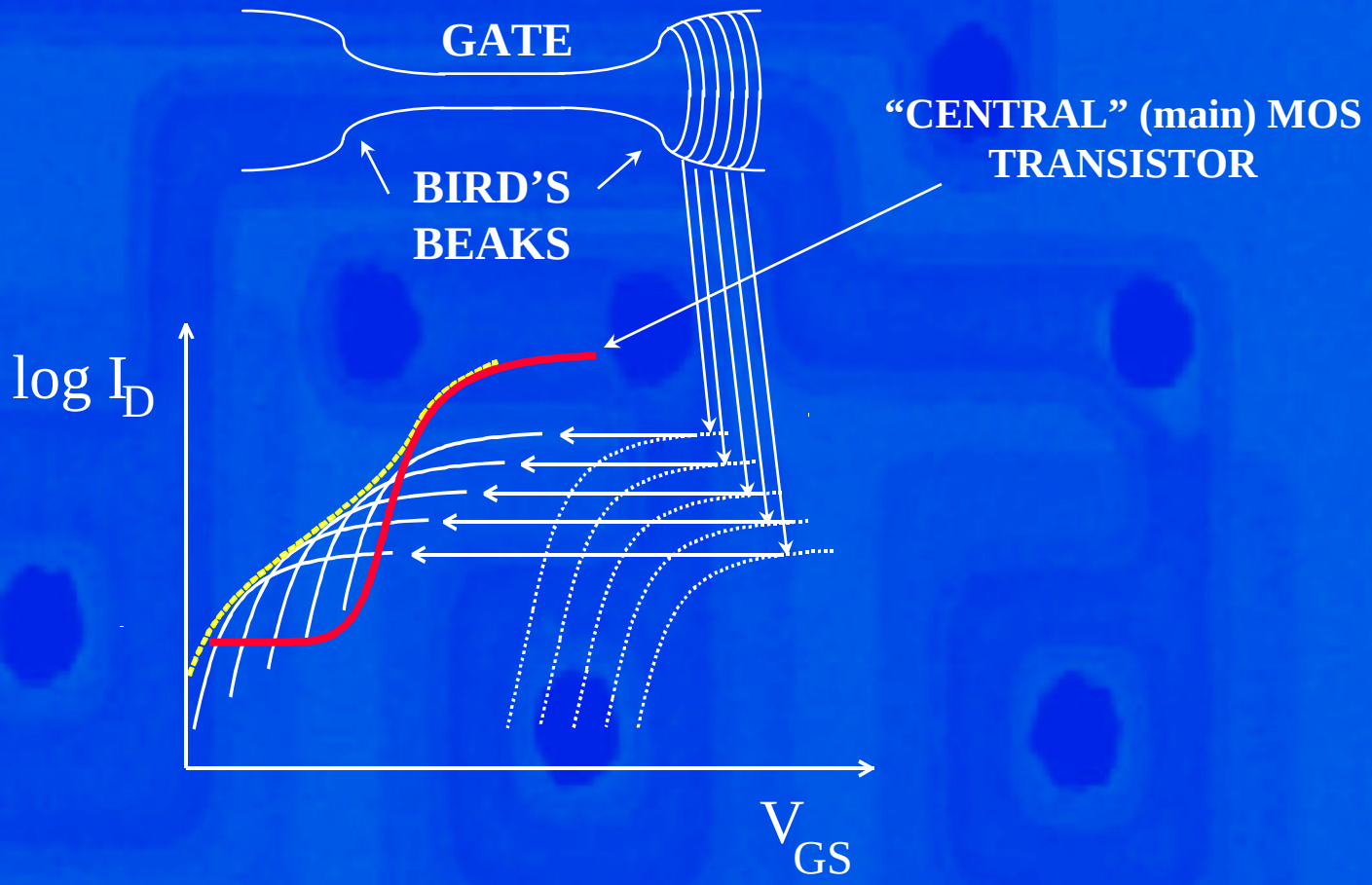
Transistor level leakage





Transistor level leakage

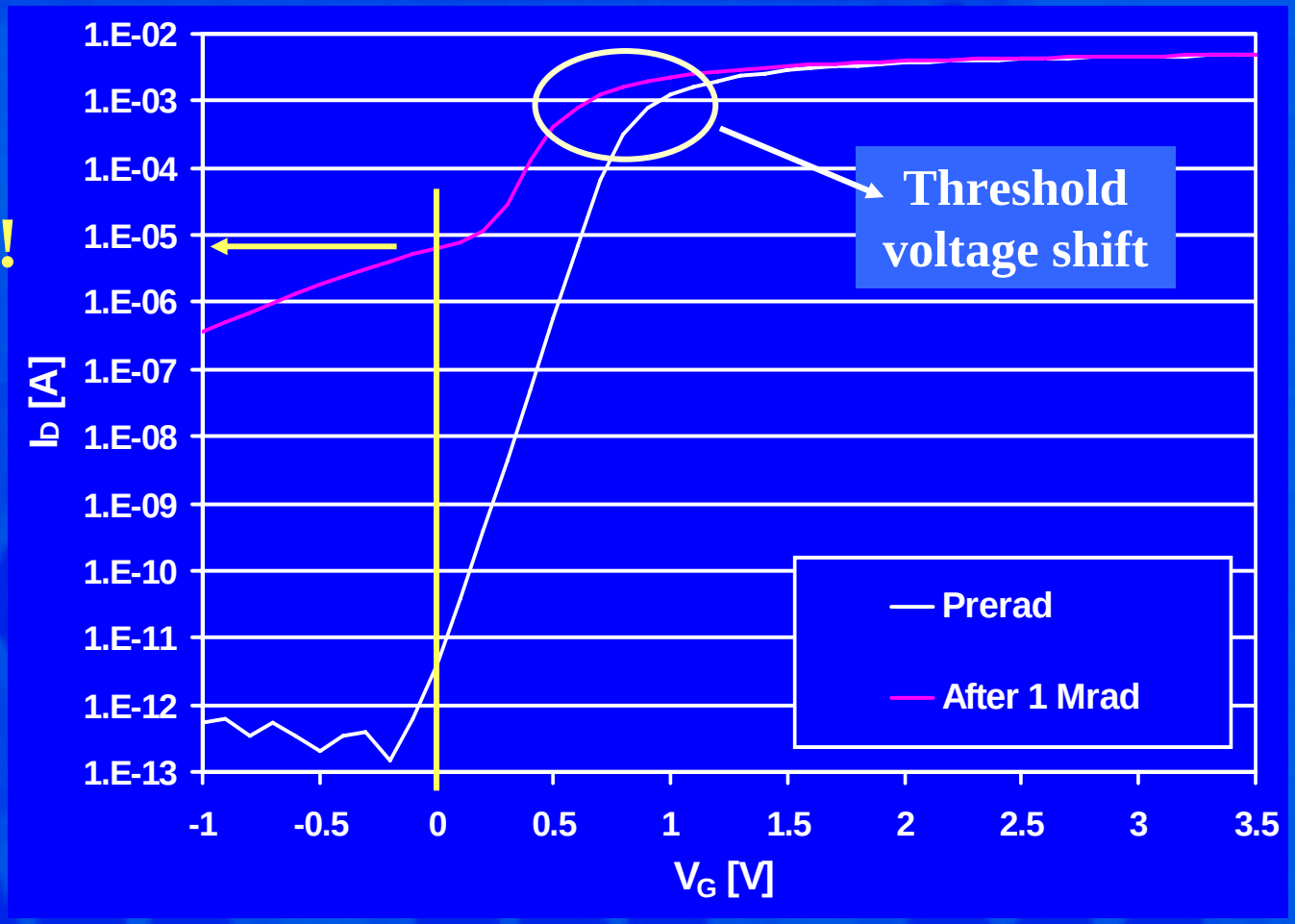
This is for LOCOS, very similar for STI



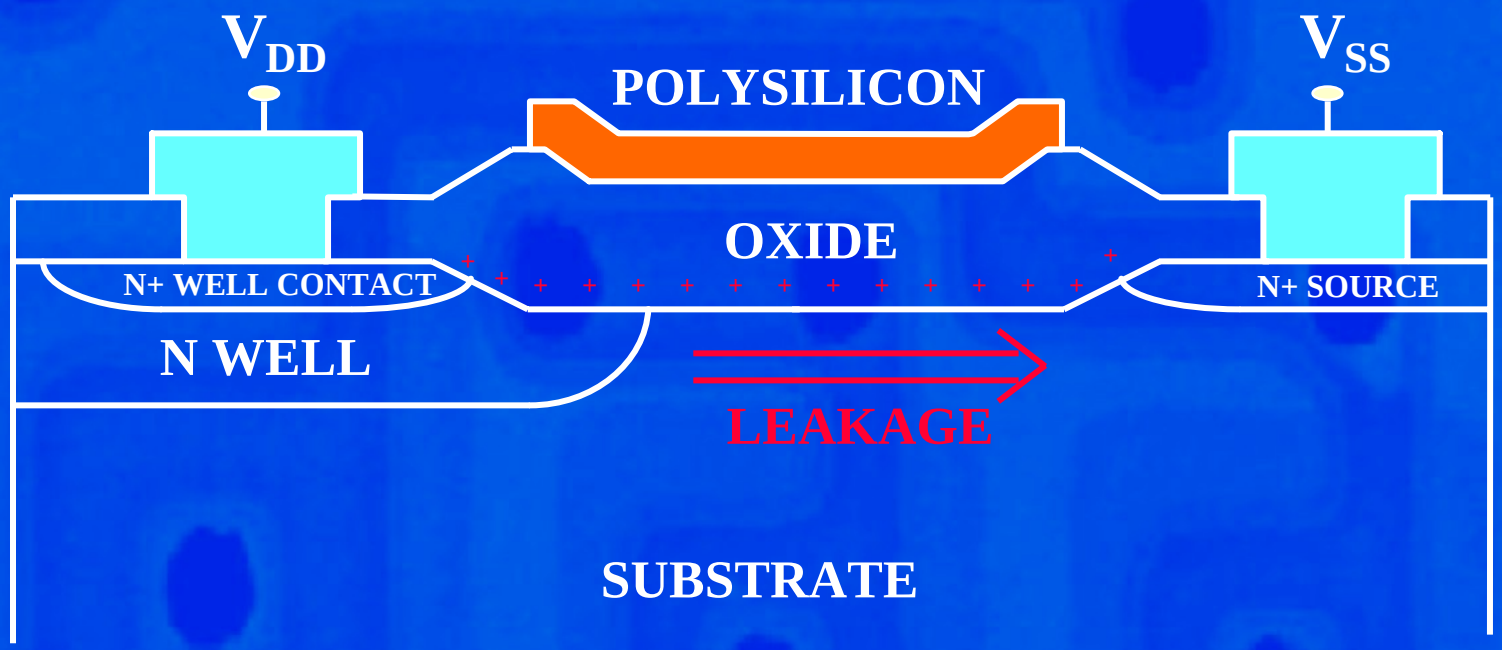
Transistor level leakage: example

NMOS - 0.7 μm technology - t_{ox} = 17 nm

μA!



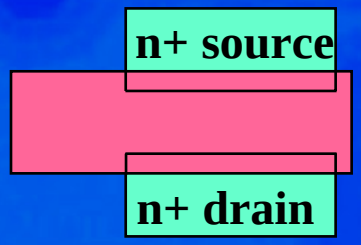
IC level leakage



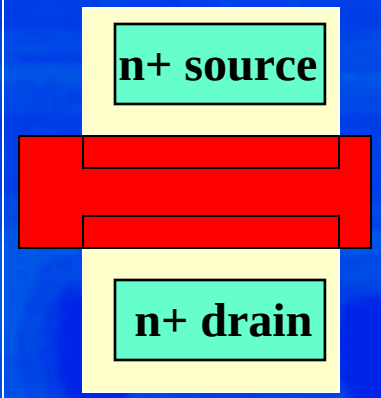
The charges trapped in the thick oxide (LOCOS or STI) decrease the Vth of the MOS structure, and the p substrate can be inverted even in the absence of an electric field. A leakage current can appear.

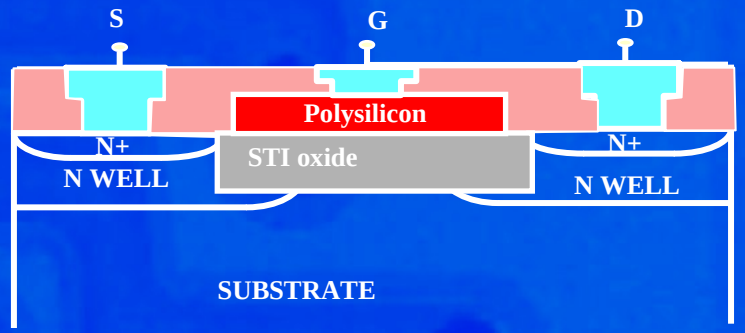
IC level leakage - FoxFETs

Between n+ diffusions

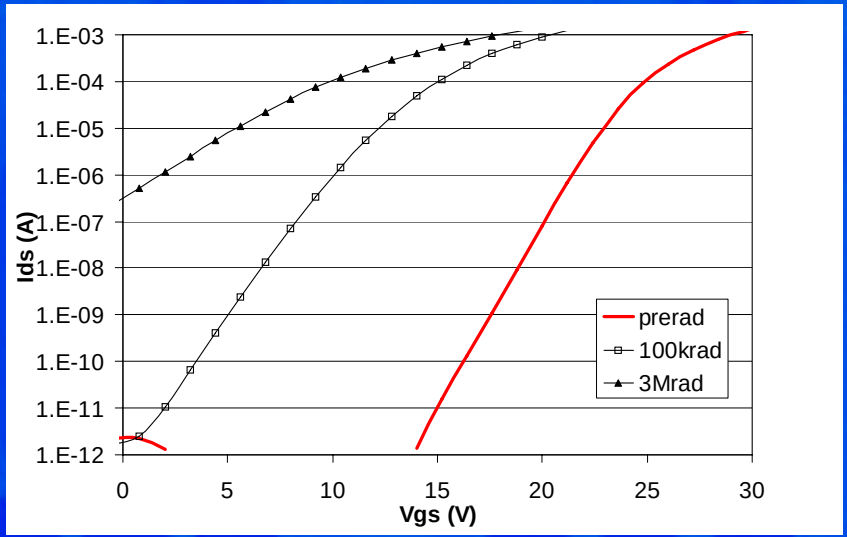


Between nwells



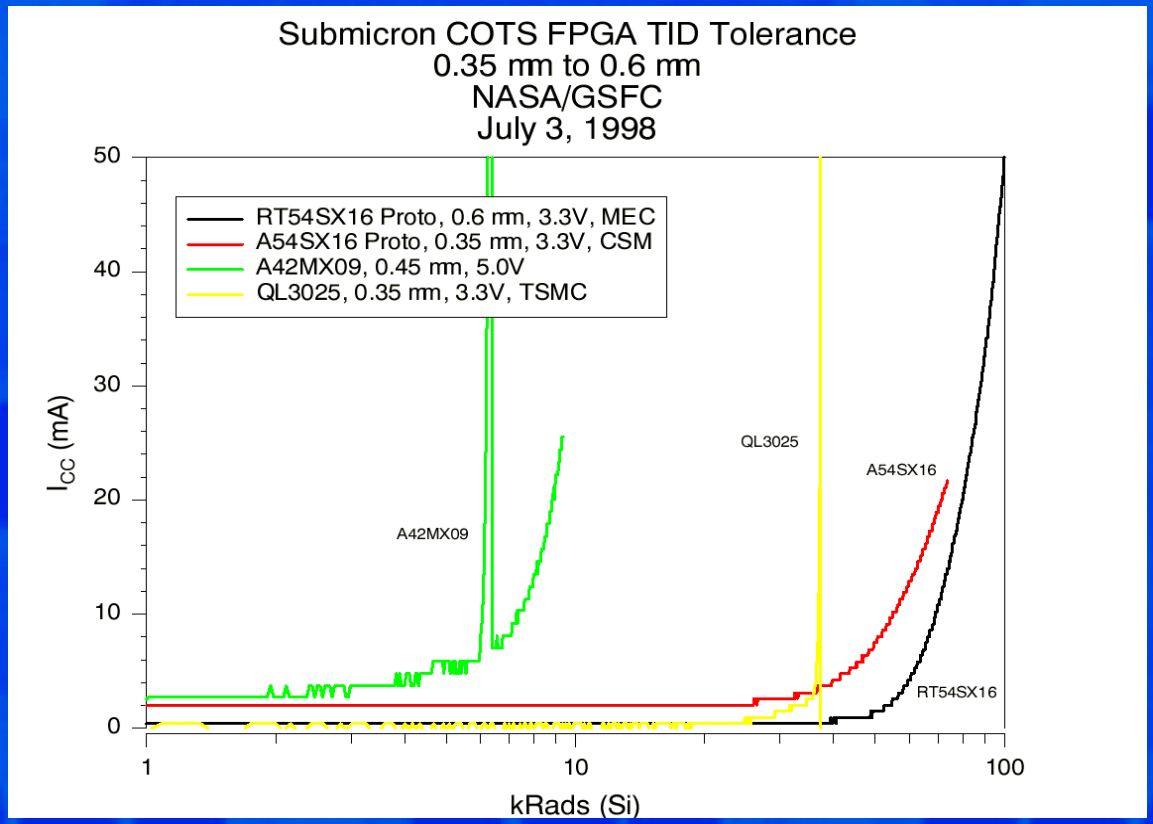


Example:
FOXFET nwell-nwell
Techno 130nm CMOS
W/L=200/0.92um



TID-induced failure

- ✓ In modern technologies, leakage current is typically the killer



TID in CMOS

Summary of the problems

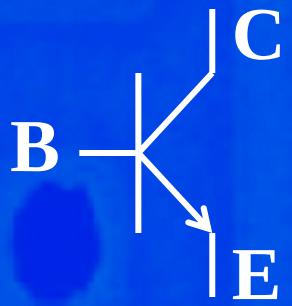
- ✓ Main transistor:
  - Threshold voltage shift, transconductance and noise degradation
  - Effects get negligible in modern deep submicron (as from 250-180 nm techs)
- ✓ Parasitic leakage paths:
  - Source – drain leakage
  - Leakage between devices
  - This are still potentially deleterious – although things looks to be better as from 130nm techs

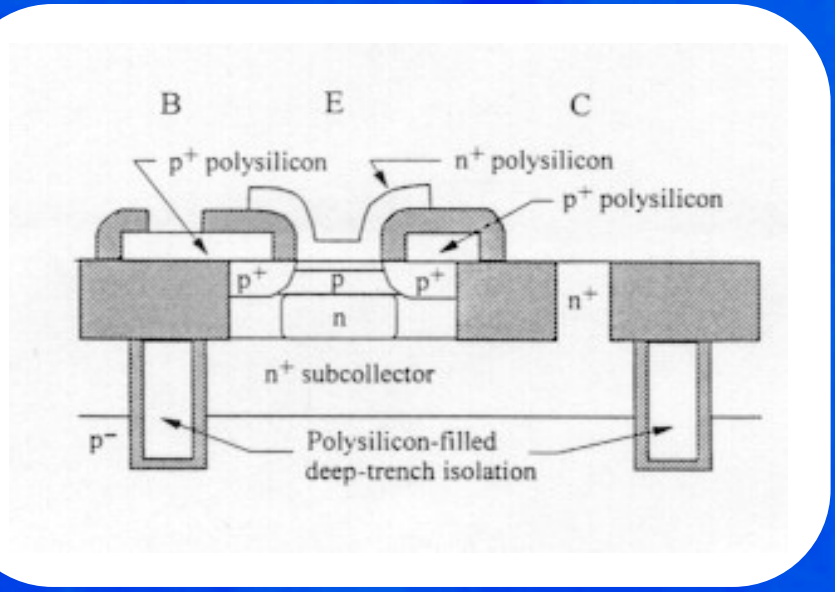
Radiation effects in devices and technologies

Outline

- ✓ General view
- ✓ Total Ionizing Dose (TID)
  - TID in CMOS technologies
  - TID in bipolar technologies
- ✓ Displacement damage
- ✓ Single Event Effects
  - SEU, SET
  - Destructive events

Bipolar transistors



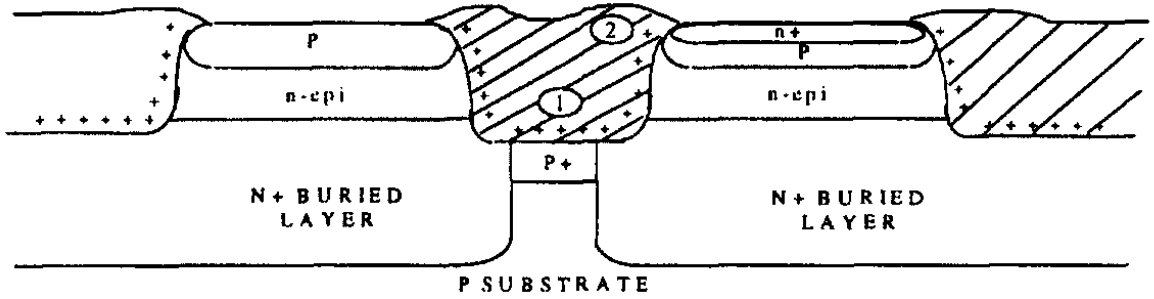


Current Gain = $\beta = I_C / I_B$

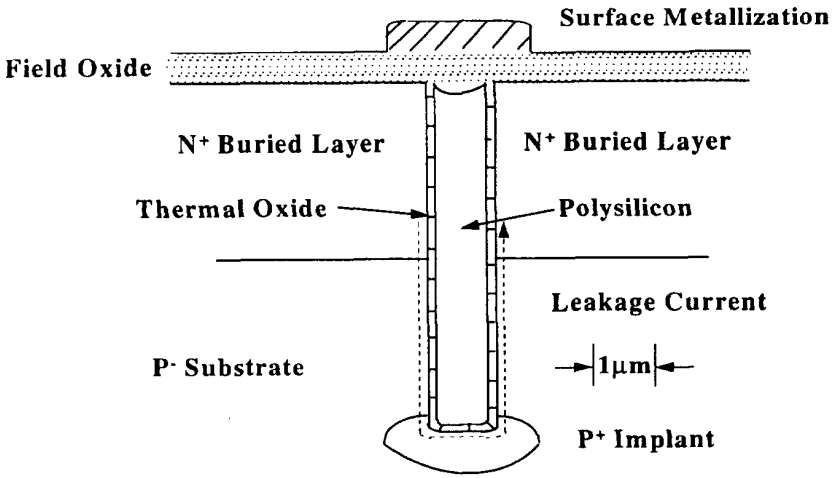
$g_m = I_C/\phi_t$

TID in bipolar devices

Substrate, sidewall and surface inversion (in oxide-isolated processes)



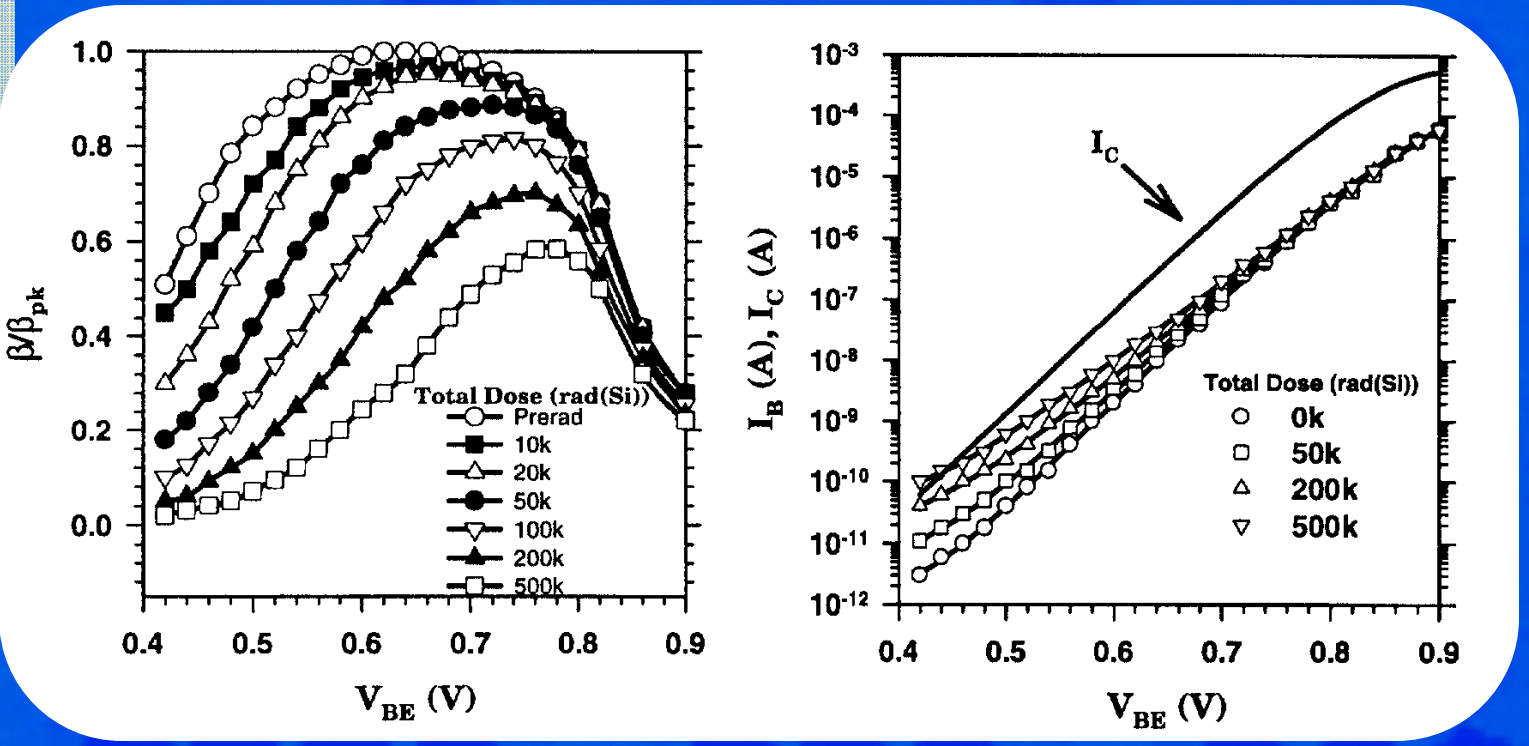
R.L.Pease et al., IEEE Trans. Nucl. Science. Vol.32, N.6, 1985



E.W.Enlow et al., IEEE Trans. Nucl. Science. Vol.36, N.6, 1989

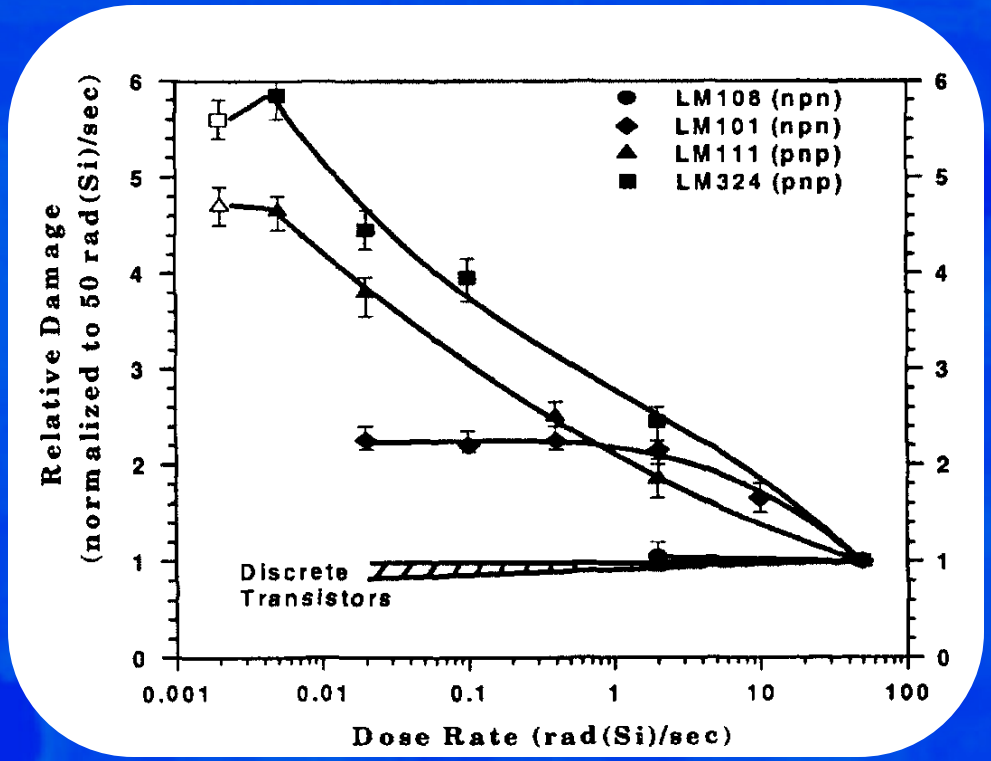
TID in bipolar devices

Gain degradation:
Increase of the surface component of the base current



R.N.Nowlin et al., IEEE Trans. Nucl. Science. Vol.39, N.6, 1992

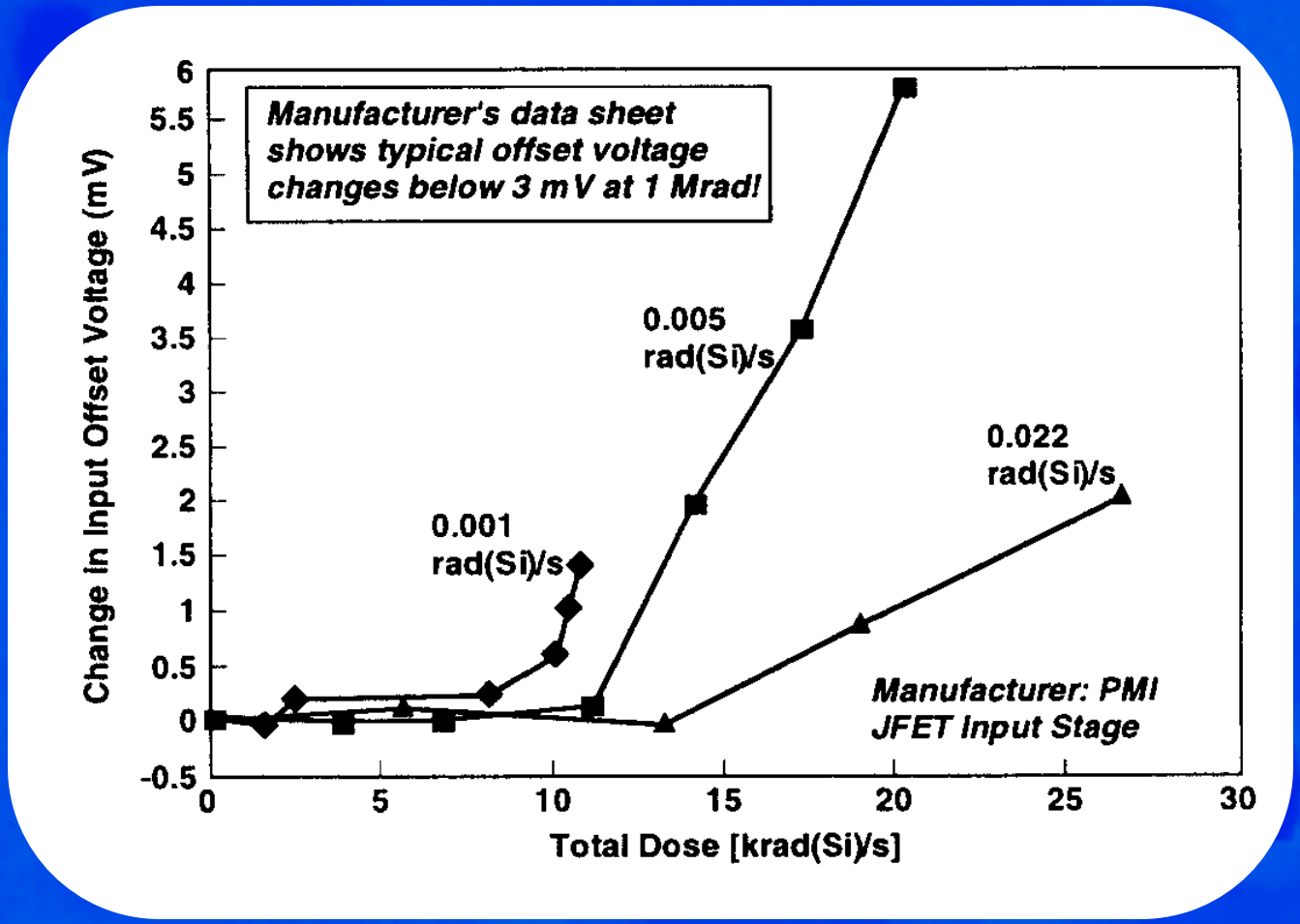
Low dose rate (LDR) effect



A.H.Johnston et al., IEEE Trans. Nucl. Science. Vol.41, N.6, 1994

Summary: LDR appears to be consistently inconsistent

Examples of LDR effects



A.H.Johnston et al., JPL internal report, 1999

LDR: possible test procedures

- ✓ High temperature test (also advised by JPL, but for TID above 30krad)
- ✓ JPL advice:

TID_{spec} < 30krad	TID_{spec} > 30krad
50 & 0.005 rad/s test at room T compare if failure in any condition (@TID<1.5TID_{spec}) => do not use!	test up to 30krad in 3 conditions: 50 & 0.005 rad/s at room T, 1rad/s at 90°C compare if comparable => use 90°C test BUT take an additional SF = 2 on TID_{spec}

Radiation effects in devices and technologies

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- ✓ General view
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- ✓ Single Event Effects
  - SEU, SET
  - Destructive events

Displacement damage: sensitive devices

- ✓ Bipolar linear ICs
- ✓ Optocouplers
- ✓ Some type of optical sources
- ✓ Optical detectors

Displacement in bipolar devices

✓ Gain degradation due to increased recombination of minority carriers in the base

Displacement damage equation:

$$1/h_{FE} - 1/h_{FE0} = \Phi / [K(2\pi f_T)]$$

NB: The majority of linear ICs are still manufactured in old junction-isolated processes, BUT using less conservative approaches (more PNP transistors used in critical places)

✓ Results on biased and unbiased devices are almost identical

Bipolar technologies

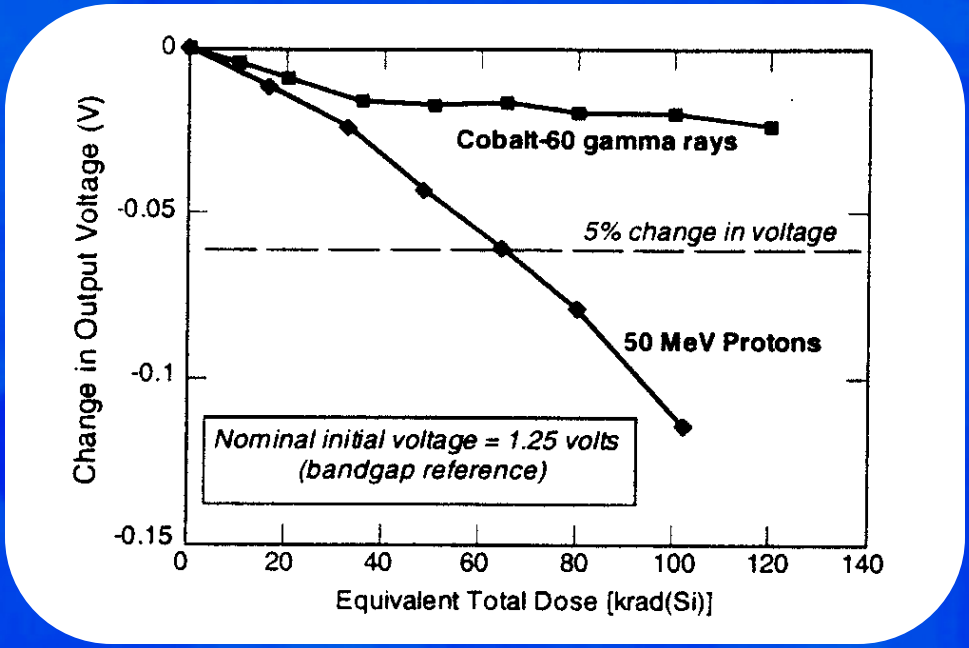
TID
Leakage paths and β degradation
Sensitive with dose rate effects
Variable failure levels

Simultaneous effects:
they add up

Displacement damage
β degradation
Voltage regulators, comparators, op amps

Displacement in bipolar devices: example

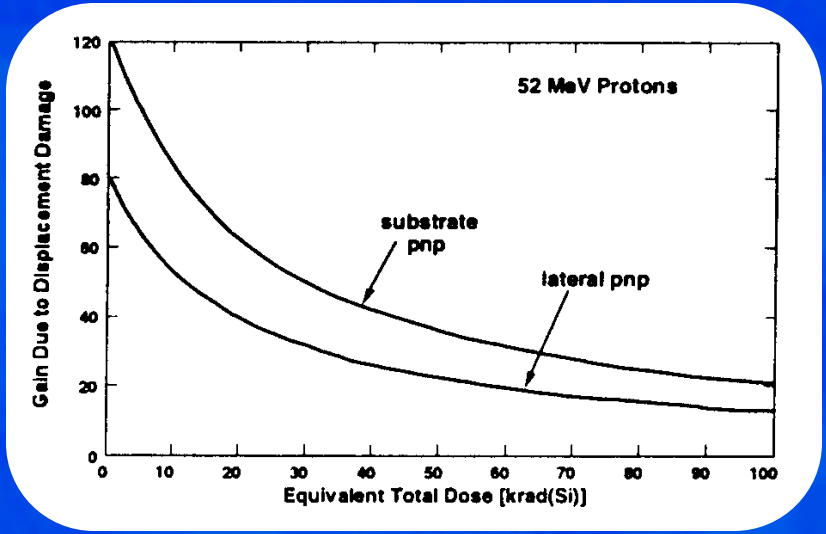
LM117 positive voltage regulator; effect of TID and displacement add up!



B.G.Rax et al., to be published in IEEE Trans. Nucl. Science, Vol.46, n.6, December 1999

Displacement in bipolar devices

Effects for lateral and substrate PNP



B.G.Rax et al., to be published in IEEE Trans. Nucl. Science, Vol.46, n.6, December 1999

B.G.Rax et al., to be published in IEEE Trans. Nucl. Science, Vol.46, n.6, December 1999

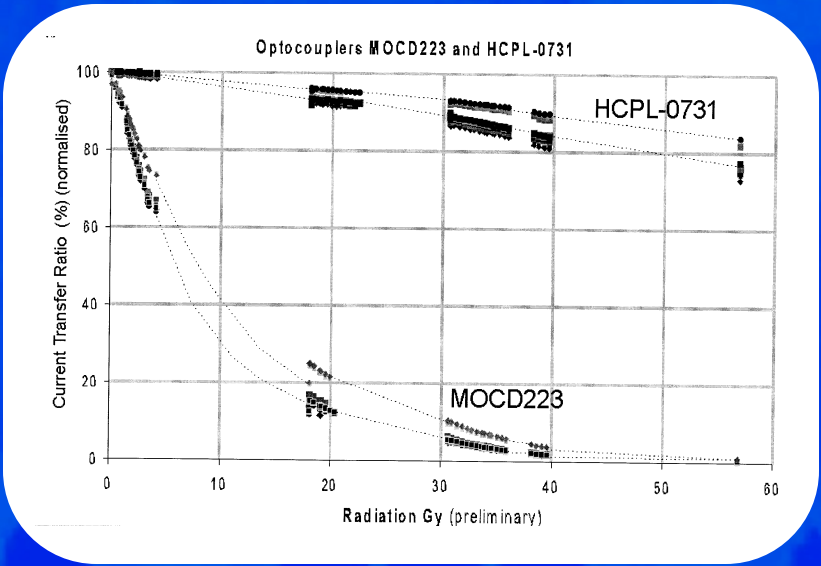
Displacement damage effects are generally negligible below $3 \cdot 10^{10}$ p/cm^2 (50MeV) also for PNP transistors

At levels above about $3 \cdot 10^{11}$ p/cm^2 , they start to become significant also for NPN transistors

Displacement for optocouplers: example

Radiation tests of the ATLAS DCS front-end electronics at the CERN TCC2 area for the CAN Fieldbus - B. Hallgren

MOCD223 from Motorola => normalized CTR 0.65%
HCPL-0731 from HP => normalized CTR 77%
ILD206A from Siemens => normalized CTR 3.5%



B.Hallgren, CERN, 1999

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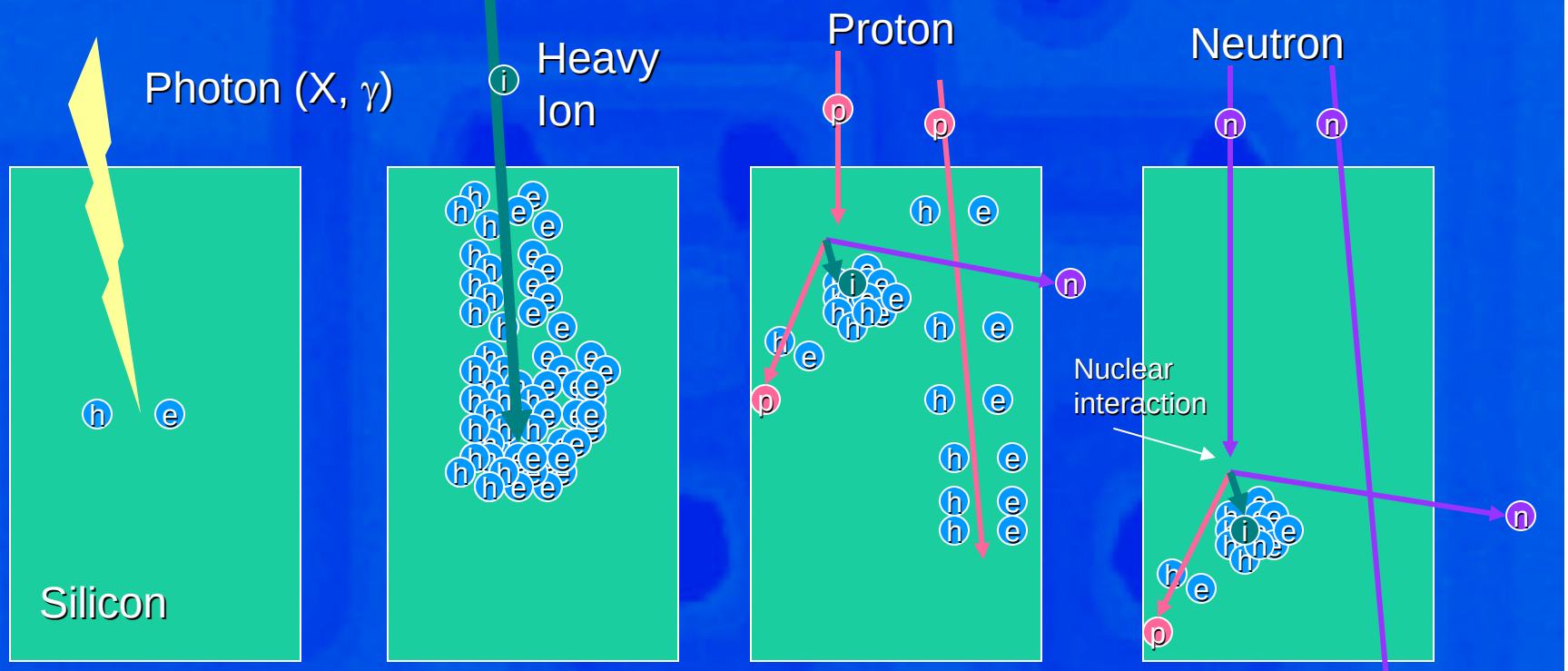
Ionization from different radiation

- ✓ Traceable to the energy deposition initiated by one single particle, in a precise instant in time. Due to its stochastic nature, this can happen at any time – even at the very beginning of the irradiation
- ✓ Which particles can induce SEEs? In the figure below, a schematic view of the density of e-h pairs created by different radiation is shown.



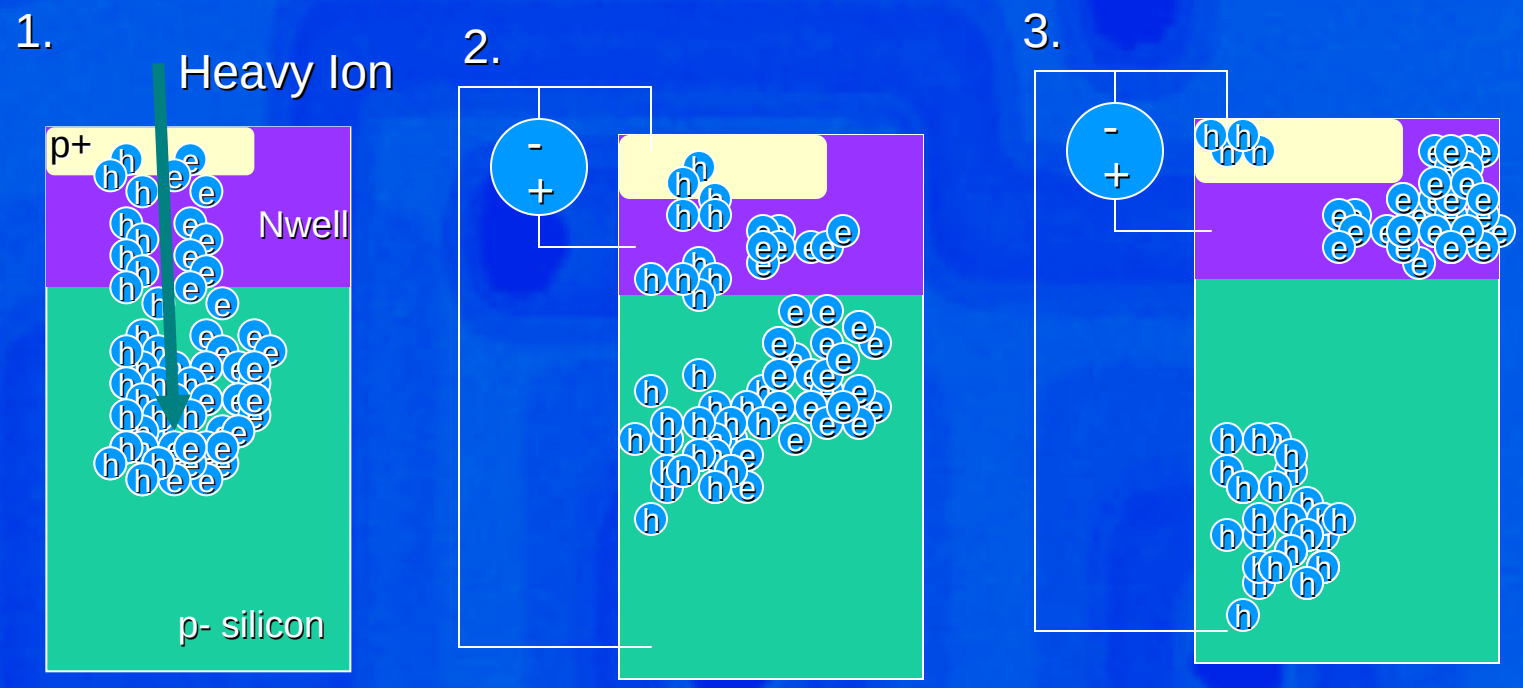
Small density of e-h pairs

Large density of e-h pairs

Small (proton) or no (neutron) density for direct ionization. Possible high density from Heavy Ion produced from nuclear interaction of the particle with Silicon nucleus.

Density of e-h pairs is important (1)

- ✓ Not all the free charge (e-h pairs) generated by radiation contributes to SEEs. Only charge in a given volume, where it can be collected in the relevant amount of time by the appropriate circuit node, matters

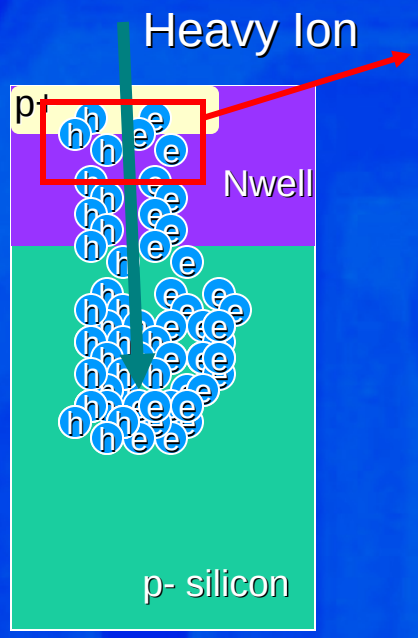


1. Ion strike: ionization takes place along the track (column of high-density pairs)

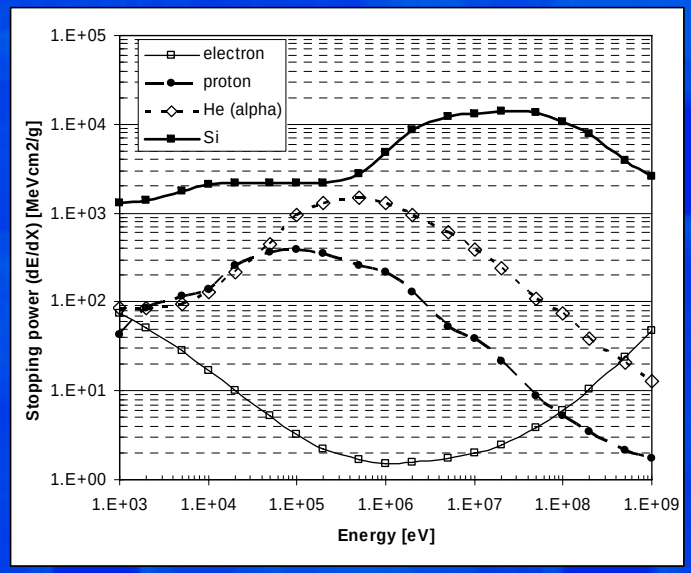
2. Charges start to migrate in the electric field across the junctions. Some drift (fast collection, relevant for SEEs), some diffuse (slow collection, less relevant for SEEs)

3. Charges are collected at circuit nodes. Note that, if the relevant node for the SEE is the p+ diffusion, not all charge deposited by the ion is collected there.

Density of e-h pairs is important (2)



Of all e-h pairs created by radiation, only those in (roughly) this volume are collected fast enough to contribute to an SEE at the node corresponding to the p+ diffusion (for instance, S or D of a PMOS FET). Density of pairs in this region determines if the SEE takes place or not! This is called the “SENSITIVE VOLUME” (SV)

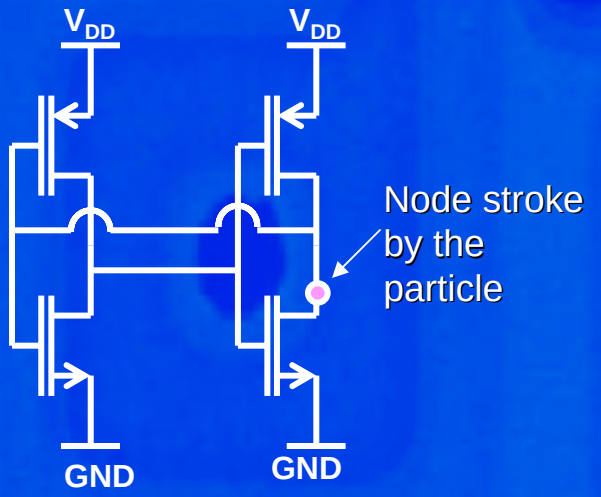


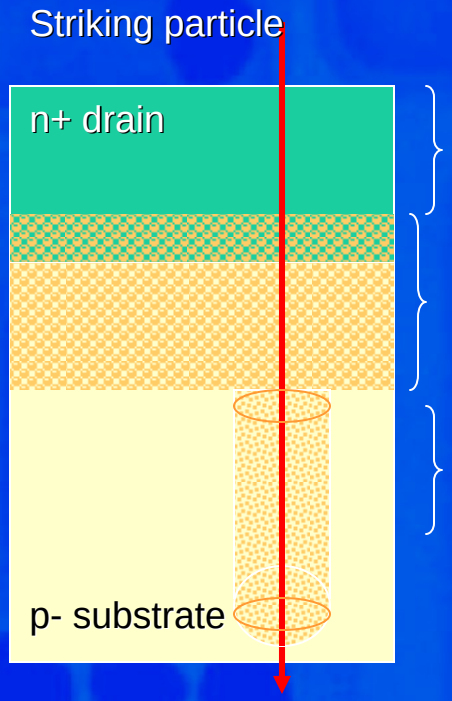
Warning: data points are approximate in this figure

The density of pairs depends on the stopping power of the particle, or dE/dx, or Linear Energy Transfer (LET). The figure above (right) shows this quantity in Si for different particles. Even protons, at their maximum stopping power, can not induce SEE in electronics circuits. Only ions, either directly from the radiation environment or from nuclear interaction of radiation (p, n, …) in Silicon can deposit enough energy in the SV to induce SEEs.

Single Event Upset (SEU) (1)

The e-h pairs created by an ionizing particle can be collected by a junction that is part of a circuit where a logic level is stored (logic 0 or 1). This can induce the “flip” of the logic level stored. This event is called an “upset” or a “soft error”.
This typically happens in memories and registers. The following example is for an SRAM cell.





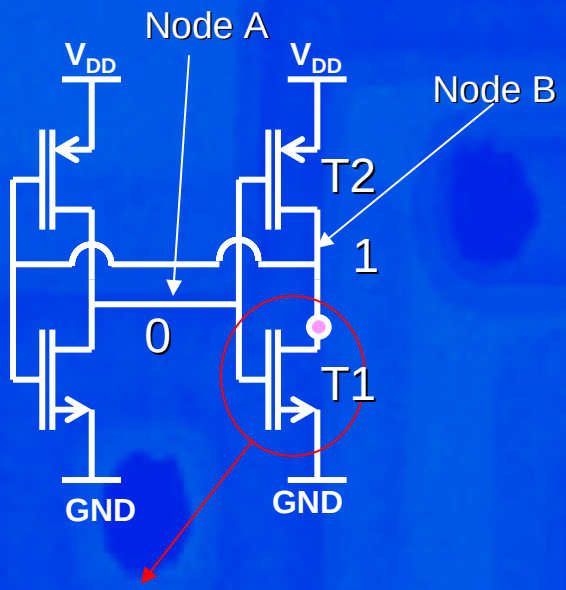
e-h pairs in this region recombine immediately (lots of free electrons available in this n+ region)

Depletion region: e-h pairs are collected by n+ drain and substrate => those collected by the drain can contribute to SEU

High density of e-h pairs in this region can instantaneously change effective doping in this low-doped region, and modify electric fields. This is called “funneling”. Charge can hence be collected from this region to the n+ drain, although a portion of it will arrive “too late” to contribute to SEU

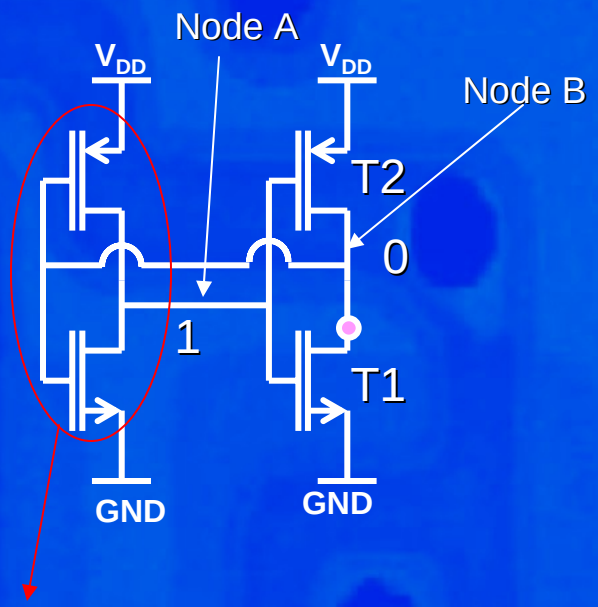
Single Event Upset (SEU) (2)

1. Initial condition
(correct value stored)



Charge collected at the drain of NMOS T1 tends to lower the potential of the node B to gnd. PMOS T2 provides current from Vdd to compensate, but has a limited current capability. If the collected charge is large enough, the voltage of node B drops below Vdd/2

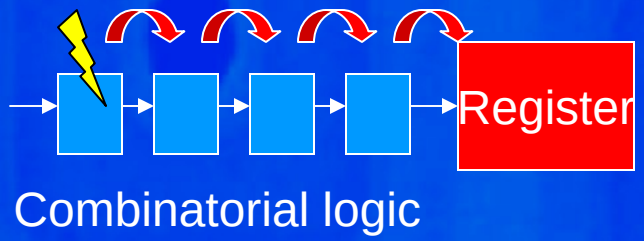
2. Final condition
(wrong value stored)

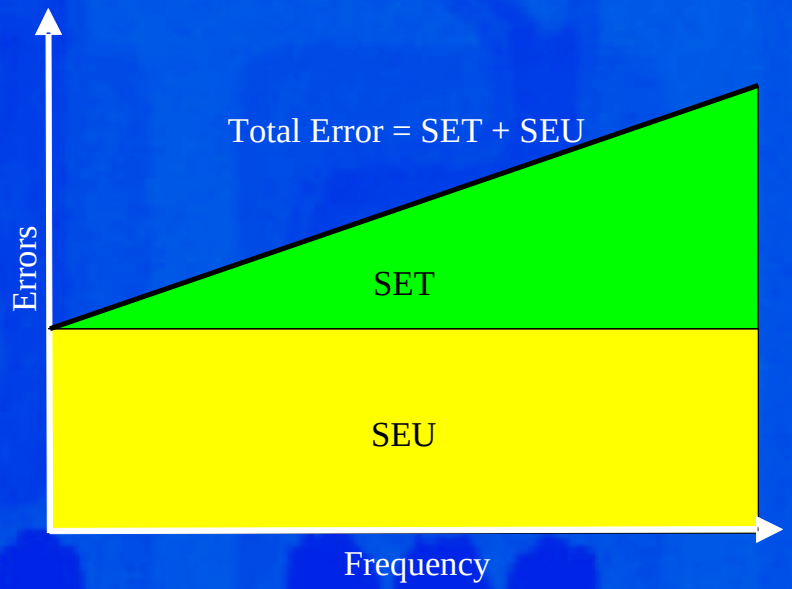


When node B drops below Vdd/2, the other inverter in the SRAM cell changes its output (node A) to logic 1. This opens T2 and closes T1, latching the wrong data in the memory cell.

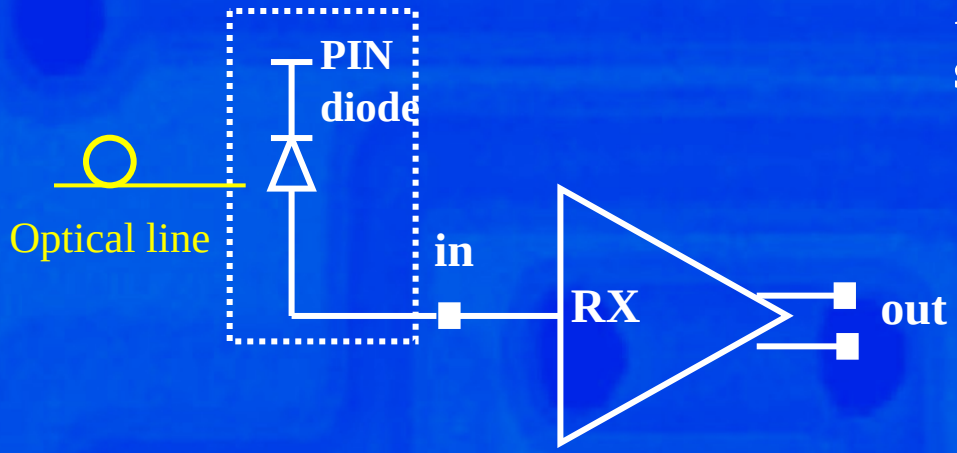
“Digital” Single Event Transient (SET)

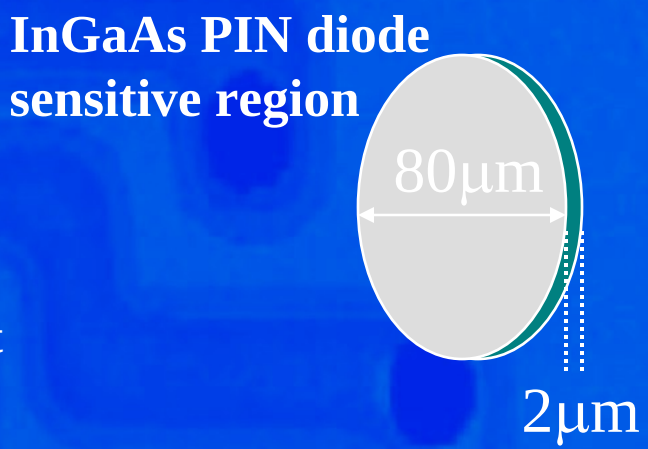
- ✓ Particle hit in combinatorial logic: with modern fast technologies, the induced pulse can propagate through the logic until it is possibly latched in a register
- ✓ Latching probability proportional to clock frequency
- ✓ Linear behaviour with clock frequency is observed

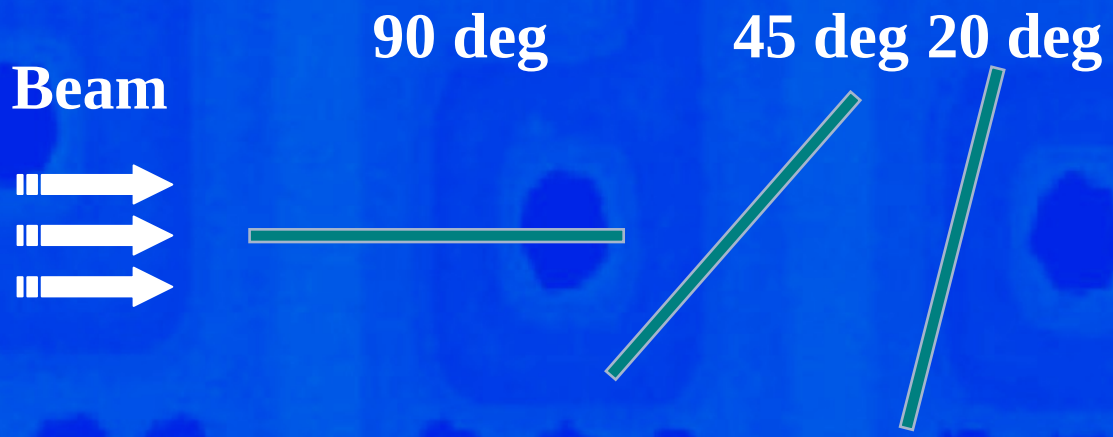




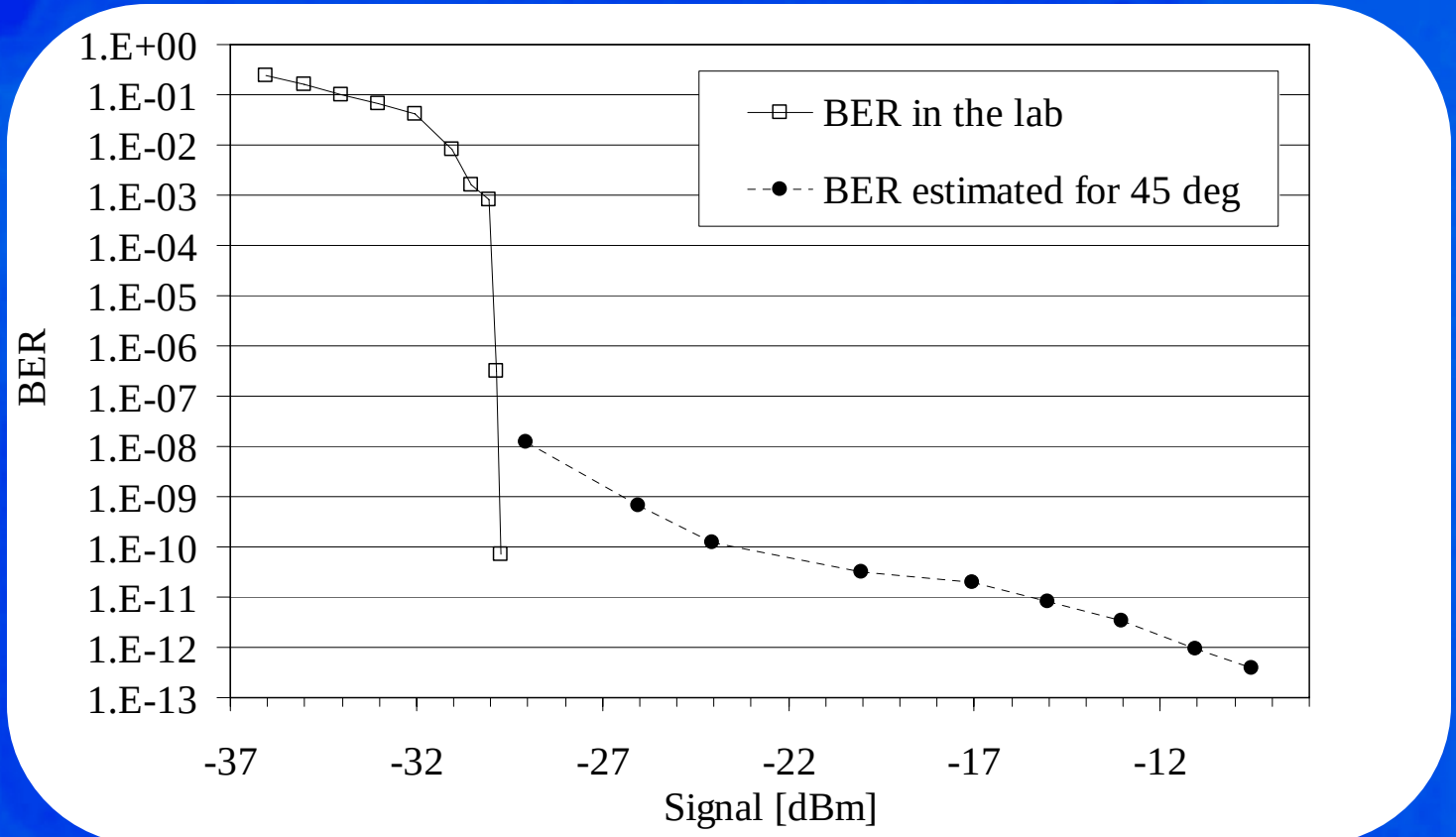
“SEU” in optical receivers (1)







“SEU” in optical receivers (2)

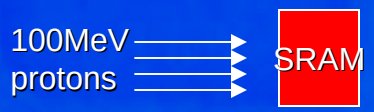


SEU cross-section (1)

- ✓ Sensitivity of a circuit to SEU (or in general to any SEE) is characterized by a cross-section
- ✓ The cross-section contains the information about the probability of the event in a radiation environment

Example: what is the error rate of an SRAM in a beam of 100MeV protons of flux 10^5 p/cm^{2}s?

1. Take the SRAM and irradiate with 100MeV proton beam. To get good statistics, use maximum flux available (unless the error rate observed during test is too large, which might imply double errors are not counted => error in the estimate)



2. Count the number of errors corresponding to a measured fluence (=flux x time) of particles used to irradiate

Example:
N of errors = 1000
Fluence = 10^{12} p/cm^2

Cross-section (σ)= N/F = 10^{-9} cm^2

3. Multiply the cross-section for the estimated flux of particles in the radiation environment. The result is directly the error rate, or number of errors per unit time.

If (σ) = 10^{-9} cm^2

and flux = 10^5 p/cm^{2}s

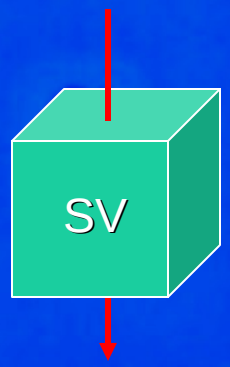
Error rate = 10^{-4} errors/s

SEU cross-section (2)

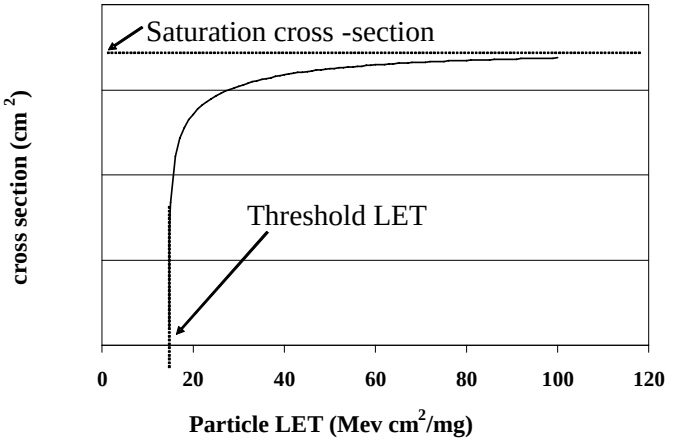
- ✓ In reality, things are generally more difficult – the real radiation environment is a complex field of particles
- ✓ One needs models to translate cross-sections measured at experimental facilities (protons or heavy ions beams) into error rates in the field
- ✓ The better the experimenter knows the sensitivity of the circuit, the better he/she can estimate the error rate in the real environment
- ✓ Heavy Ions (HI) irradiation tests are very good to probe completely the sensitivity of a circuit. With HI, it is possible to vary the LET of the particles (hence the energy deposited in the SV), and measure the correspondent cross-section.

LET= 1 MeVcm^2/mg

Example SV: Cube with 1um sides



The path of this particle in the SV is 1um. Since the density of Si is 2.32g/cm^3, the energy deposited in the SV is about 232keV.
If the LET is changed, by changing the ion, to 5, then the deposited energy exceeds 1MeV.
It is possible to chart the measured cross-section for different LET of the ions, as shown in the figure to the right.



SEU cross-section (3)

- ✓ Heavy ions tests are more expensive and more complicated to perform (few facilities, need to expose circuit without package)
- ✓ As an alternative, for High Energy Physics applications (in particular for LHC detectors) it is possible to rely on mono-energetic proton beam data
- ✓ Given the complexity of the radiation field in the LHC experiments, a study has been carried with the help of Monte-Carlo simulation codes and main results and implications are discussed in the following

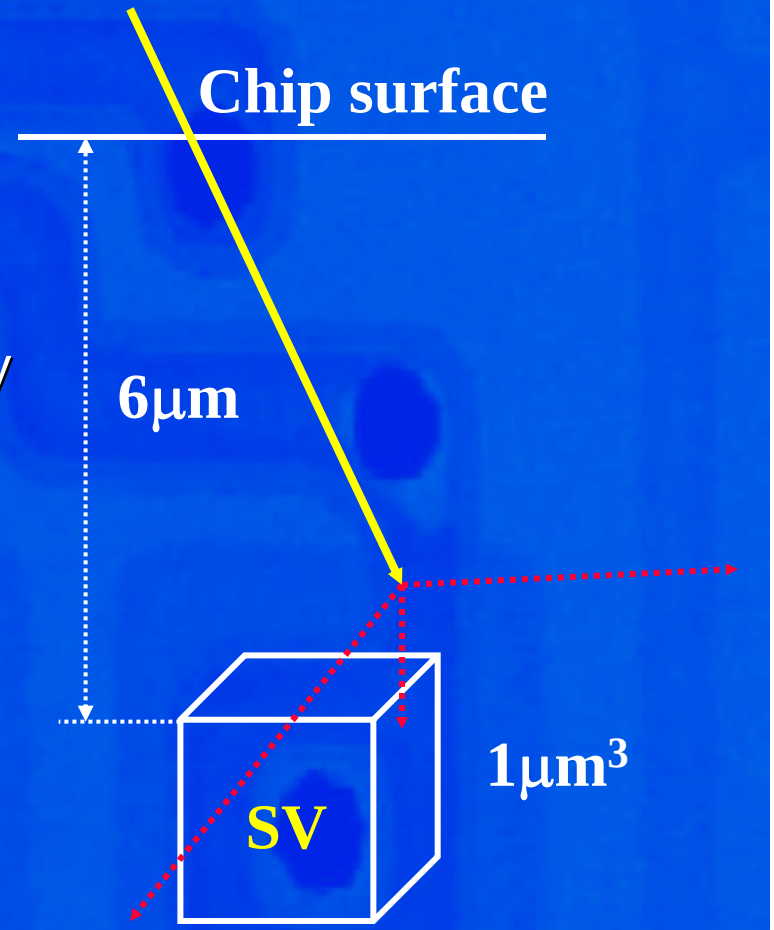
SEU rate estimate in LHC

- ✓ Hadron-dominated particle environment
- ✓ Hadrons have low LET, no “direct” SEU
- ✓ Nuclear interaction probability has to be computed, with LET and track of the fragments
- ✓ This work has been carried on in a collaboration RD49/CMS, and published
- ✓ Main conclusions highlighted here (see the following paper for more details)

M.Huhtinen, F.Faccio, “Computational method to estimate Single Event Upset rates in an accelerator environment”, Nuclear Instruments and Methods in Physics Research A 450 (2000) 155-172

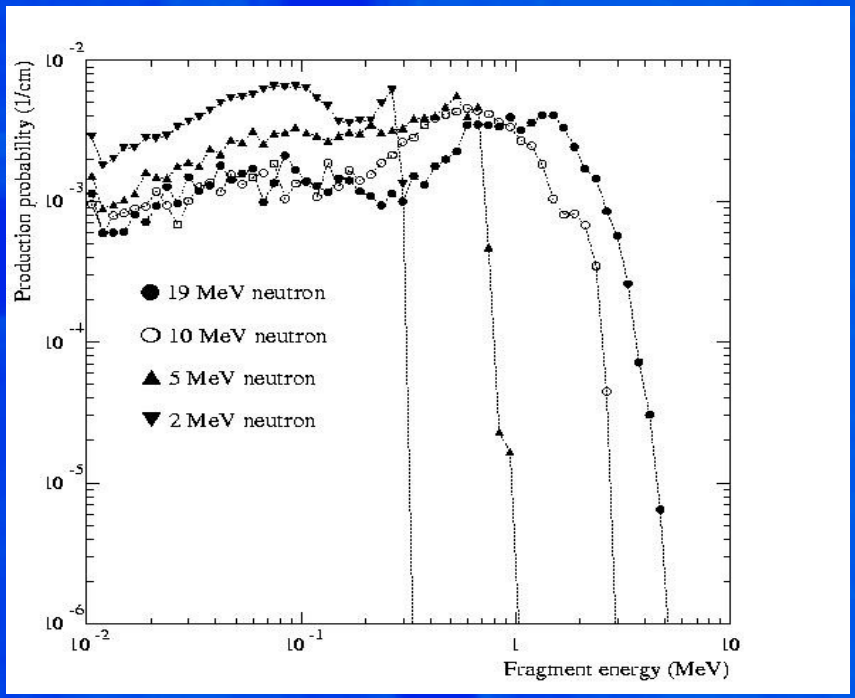
Simulation geometry & methods

- ✓ Monte-Carlo simulation approach
- ✓ Different SV shape and size used
- ✓ SV surrounded by silicon and topped by a 6μm SiO_2 layer (equivalent to Si)
- ✓ Event generators to compute the interaction probability and produced recoils
- ✓ Energy loss of all recoils computed



“Threshold energy”

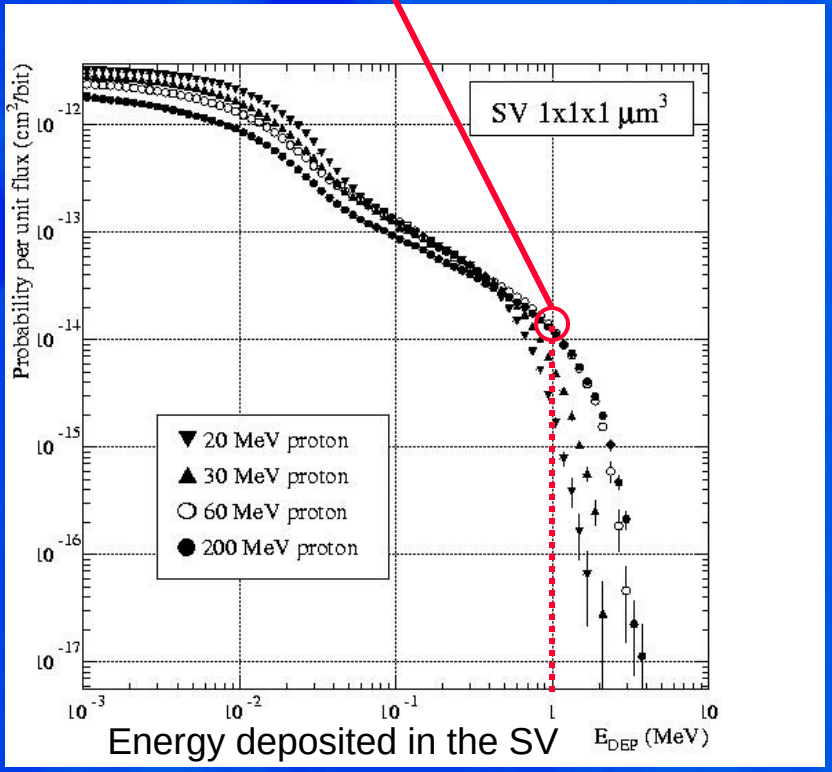
- ✓ There is a “threshold energy” of the incoming particle, below which the probability of observing an SEU drops dramatically
  - This can be easily explained when looking at the curve to the right, which depicts the probability to produce, from nuclear interaction, fragments of the energy indicated along the X axis: the lower the energy of the incoming particle (neutrons in this case), the lower the energy of the fragments – hence the lower the energy they can deposit in the SV
  - As a consequence, It is not useful – or at best difficult to exploit – to test for SEEs with beams below 50-60MeV. Nonetheless, very modern CMOS technologies that are very sensitive can have the same cross-section above some 15-20MeV, so this “threshold energy” is lower than for older technologies



Probability curves

- ✓ The main output of the simulation is a probability curve for a given SV size and a given radiation environment
  - The curve is plotted with the energy deposited in the SV as X axis (E_{dep})
  - On the Y axis, there is the probability (per unit flux and per unit SV) for any energy deposition. This contains the information on how often an energy EQUAL OR LARGER than E_{dep} is deposited in the SV
- ✓ Example of the use of one such curve
  - The curve to the right is for a SV of 1μm³ in a mono-energetic proton beam of 20, 30, 60 and 200 MeV.
  - Suppose that we have a circuit whose threshold for SEU corresponds to a deposition of 1MeV in the SV. Every time an energy equal or larger than 1MeV is deposited, the circuit has an SEU
  - The error rate in a 200MeV proton beam is the probability at E_{dep}=1MeV multiplied by the proton flux

Rate = probability x flux

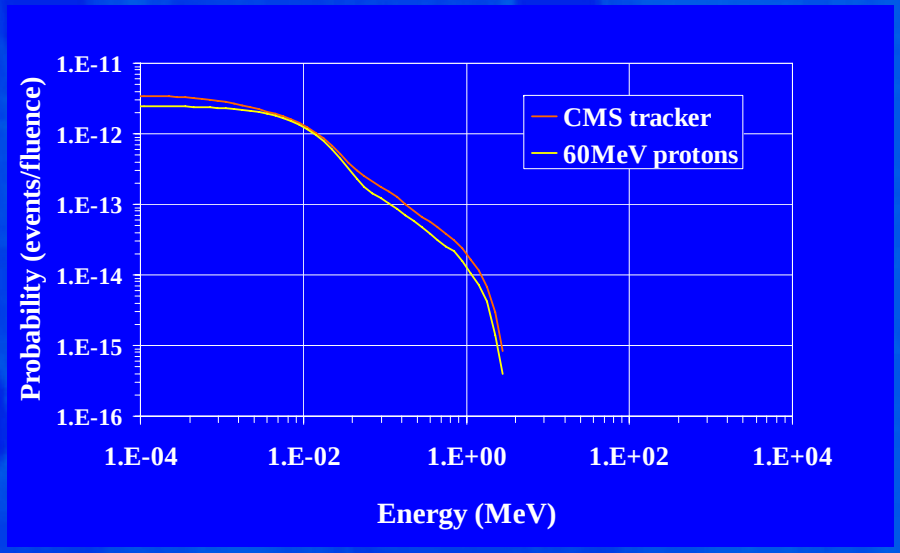


Influence of the environment

- ✓ The comparison of the probability curve for different radiation environments is very interesting
  - In the figure below, the comparison between a mono-energetic 60MeV proton beam and the complex CMS tracker environment is shown
  - The probability curves are very similar. This implies that a reasonable estimate of the error rate in the CMS tracker environment (and hence in the LHC experiments) can be obtained by measuring the cross-section of the circuit in a proton beam of at least 60MeV

- The suggested procedure for the estimate is therefore:
  1. Measure the σ in a 60MeV proton beam (or higher energy if available)
  2. Multiply the σ for the flux of particles in the LHC environment, where only hadrons above 20MeV have to be counted

  The procedure is based on the assumption, which appears reasonable from this study, that all hadrons above about 20MeV have roughly the same effect on the circuit (hence their σ is very comparable)



Conclusions of the simulation work

- ✓ Despite the large number of approximations in the model, a good agreement with available experimental data has been found
- ✓ SEU rates in LHC will in most devices be dominated by hadrons with E>20MeV. It is reasonable to assume in the estimate that all hadrons above 20MeV have the same effect
- ✓ To estimate error rates in LHC, use proton beams of 60-200MeV to measure the cross-section of the circuits. Multiply the measured s for the flux of hadrons with E>20MeV in the location where the circuit has to work. This procedure has been adopted by all LHC experiments as a "standard" for circuit qualification
- ✓ A useful information to situate the sensitivity of circuits in the LHC is the maximum LET of recoils from nuclear interaction of hadrons with the Si nuclei. The maximum LET is for a Si recoil and the LET is about 15 $MeVcm^2mg^{-1}$. This information can be used to judge if a circuit for which Heavy Ion data is available will experience a high error rate in the LHC.

Radiation effects in devices and technologies

Outline

- ✓ General view
- ✓ Total Ionizing Dose (TID)
- ✓ Displacement damage
- ✓ Single Event Effects
  - SEU, SET
  - Destructive events

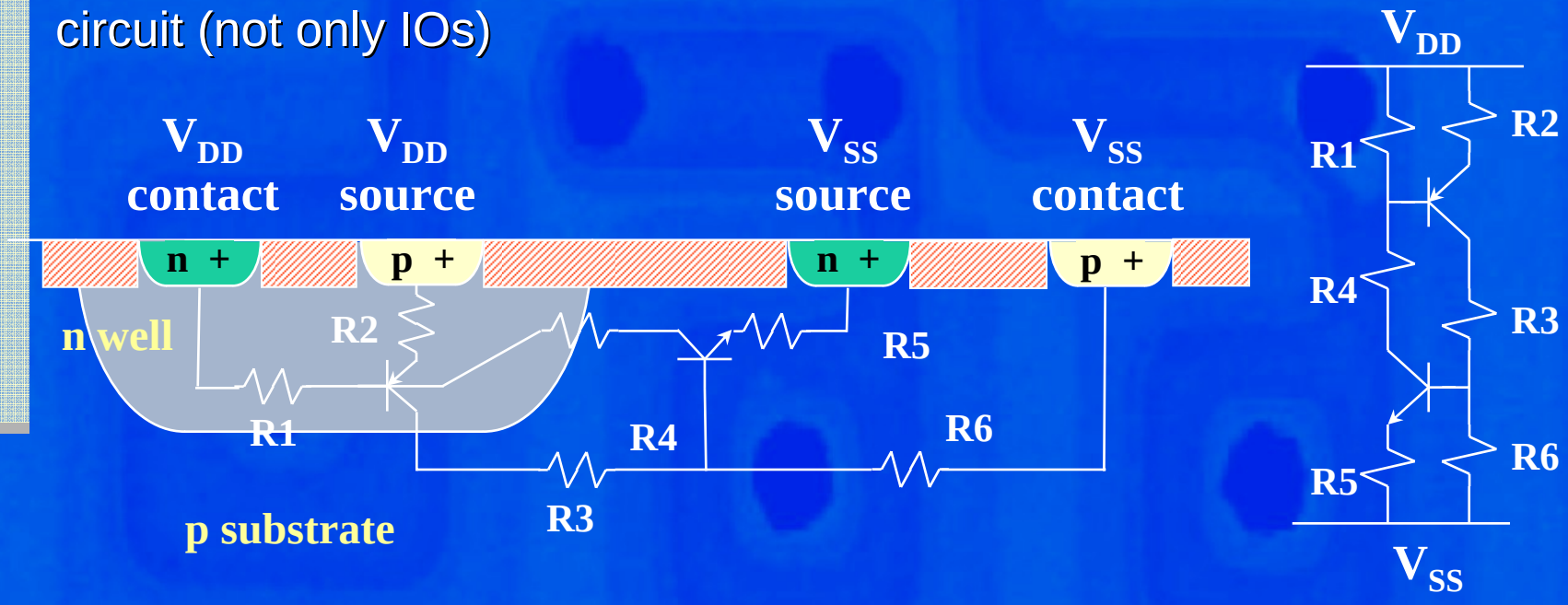
Destructive SEEs (Hard errors)

- ✓ SEBO => Single Event Burnout occurring in power MOSFET, BJT (IGBT) and power diodes
- ✓ SEGR => Single Event Gate Rupture occurring in power MOSFET
- ✓ SEL => Single Event Latchup occurring in CMOS ICs
- ✓ They can be triggered by the nuclear interaction of charged hadrons and neutrons

Single Event Latchup (SEL)

Electrical latchup might be initiated by electrical transients on input/output lines, elevated T or improper sequencing of power supply biases. These modes are normally addressed by the manufacturer.

Latchup can be initiated by ionizing particles (SEL) in any place of the circuit (not only IOs)



A.H. Johnston et al., IEEE TNS, Apr. 1996

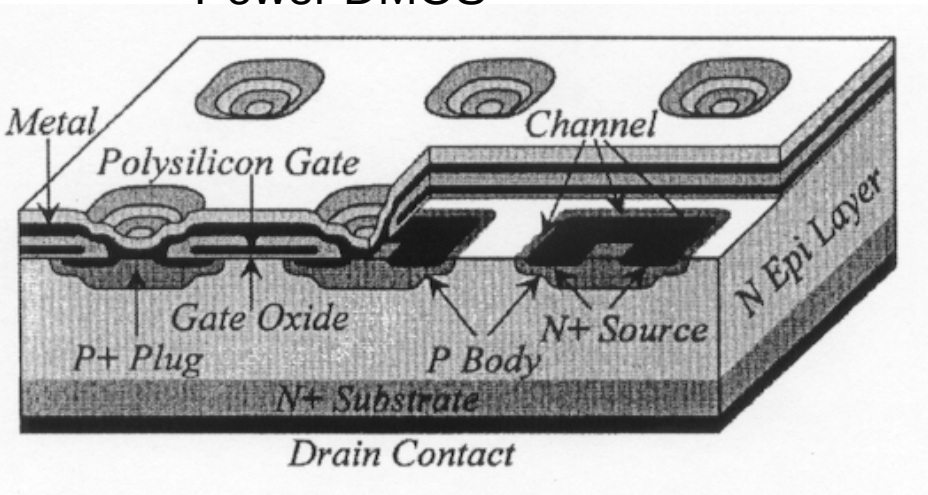
SEL: experiments

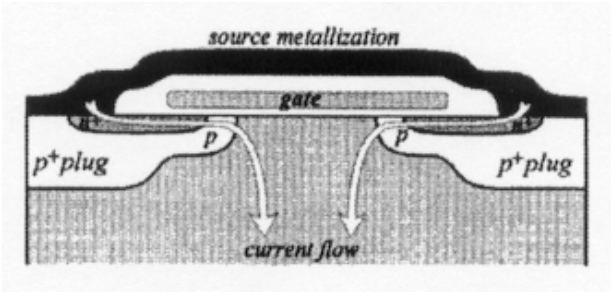
- ✓ Experiments aim at measuring the cross-section. To avoid destruction after the first occurrence, power (both core and I/Os) has to be shut off promptly upon detection of the SEL
- ✓ SEL sensitivity is enhanced by temperature, hence the test should be done at the maximum foreseen T
- ✓ Though in general modern technologies should be less sensitive to SEL, there are exceptions!
- ✓ SEL can be induced by high energy protons and neutrons
  - This is not very frequent, but in literature one can find at least 15-20 devices for which SEL was experimentally induced by proton or neutron irradiation
  - When looking at devices for which Heavy Ion data exist in literature, a rule of a thumb is: if they do not latch below an LET of 15 MeVcm^{2}mg^{-1}, they will not latch in a proton-neutron environment. In fact, typically they need to have an SEL threshold around 4 MeVcm^{2}mg^{-1} to be sensitive (but take this figure with precaution, since it is base on little statistics available…)
  - If a component is suspected to be sensitive, use high energy protons for the test (the SEL cross-section can be even 15 times larger for tests at 200MeV than for tests with 50MeV protons). Also, use a large fluence of particles for the test – at least 5x10^{10} cm^{-2} – and to enhance SEL probability increase the T during the test

SEBO (SEB)

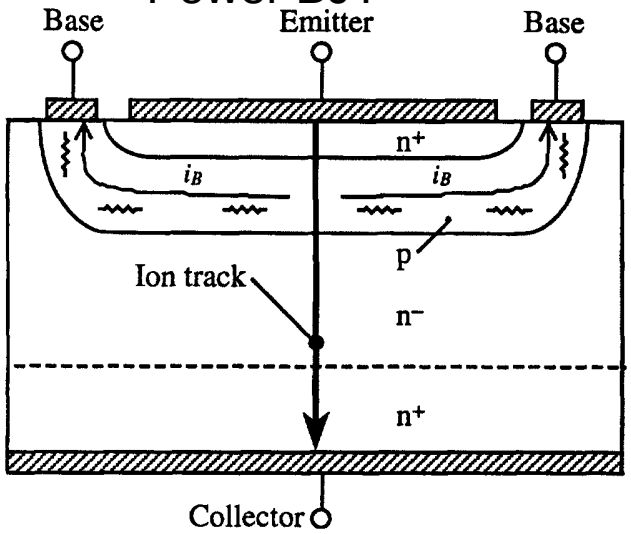
Double-diffused MOS (DMOS) power transistor and power BJT transistors are vulnerable

Power DMOS





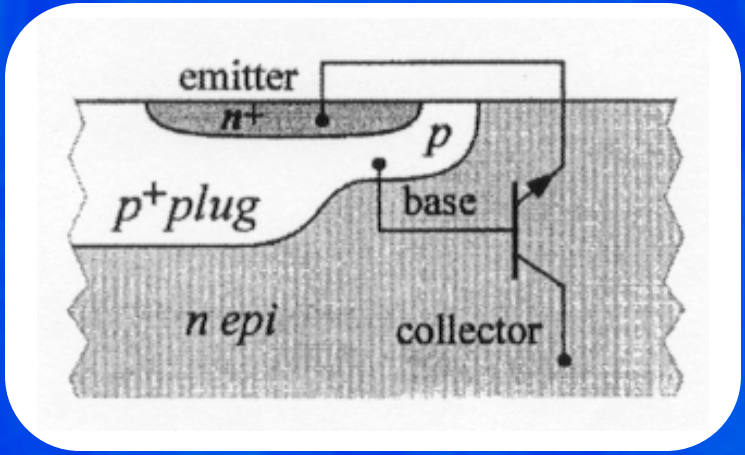
Power BJT



J.H.Johnson & K.F.Galloway, IEEE NSREC short course, 1996

SEBO (SEB)

Mechanism: passage of the ion in the OFF state, generating a transient current. A regenerative feedback occurs until second breakdown sets in and permanently destroys the device (short source-drain or emitter-collector).

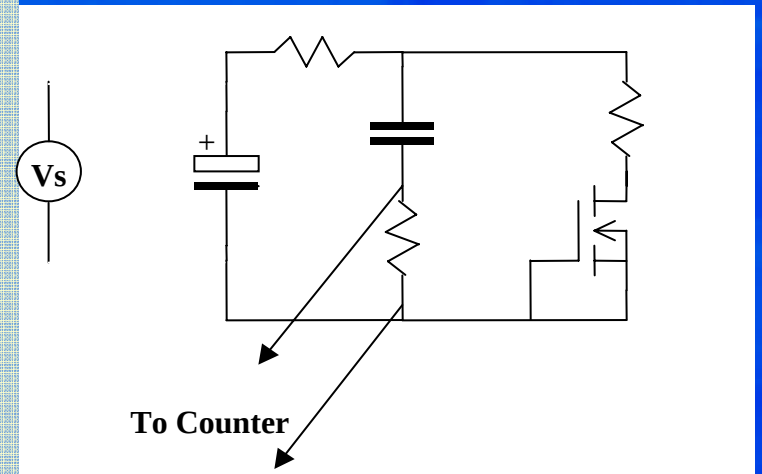


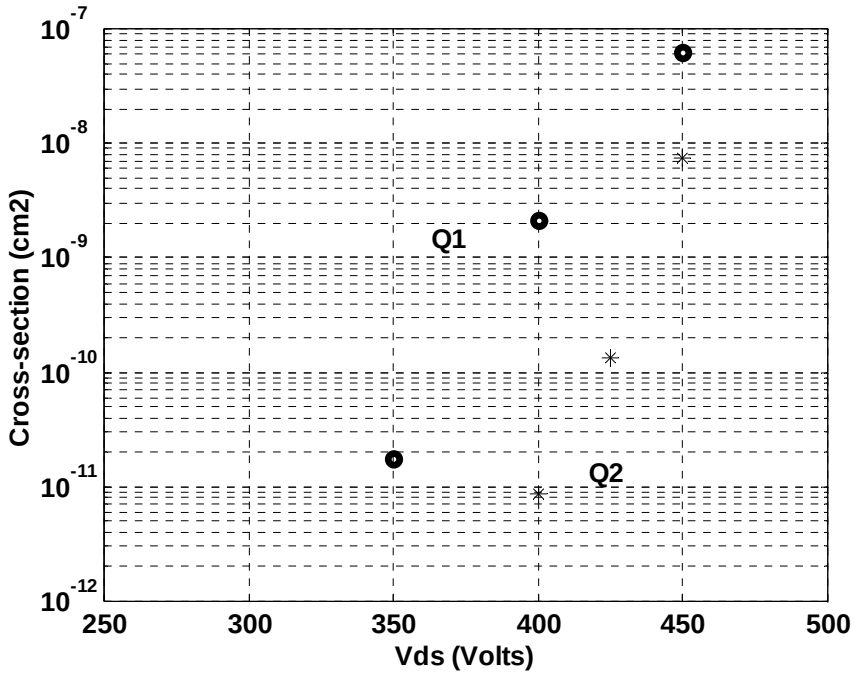
J.H.Johnson & K.F.Galloway, IEEE NSREC short course, 1996

Important mechanism in the regenerative feedback: avalanche-generated hole current in the collector region of the parasitic (or main) bipolar transistor.

SEB Example: DC-DC converter (1)

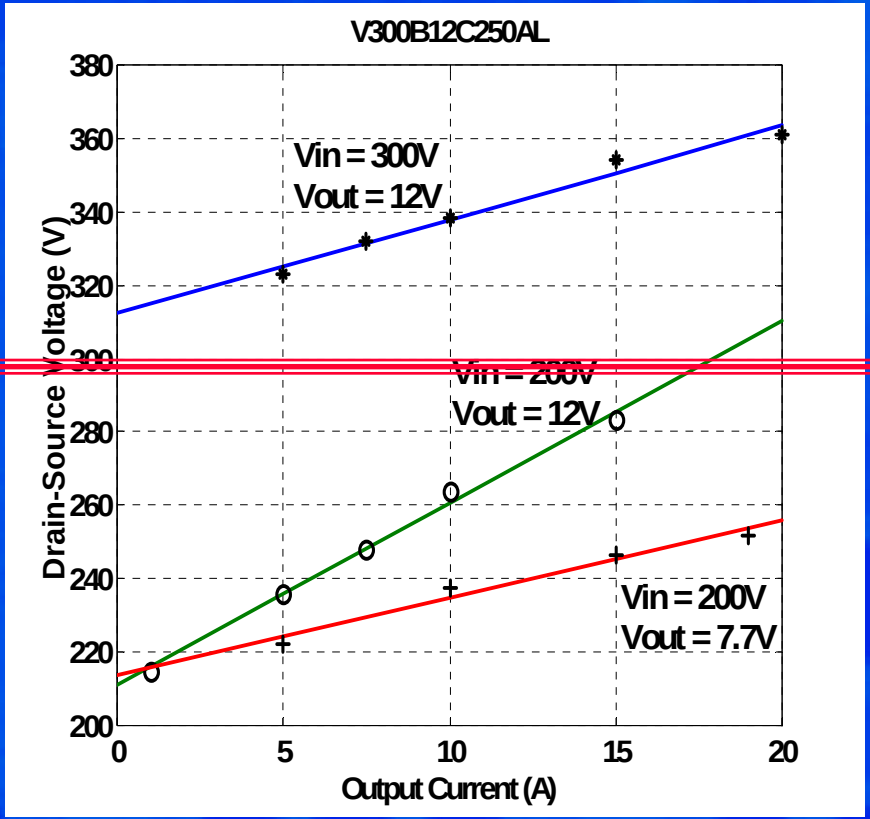
Power MOSFETs used in candidate DC-DC converter for LHC were mounted in test cards (below, left) and irradiated a different Vds with 60MeV protons. Burnout started from a Vds of about 350V.





SEB Example: DC-DC converter (2)

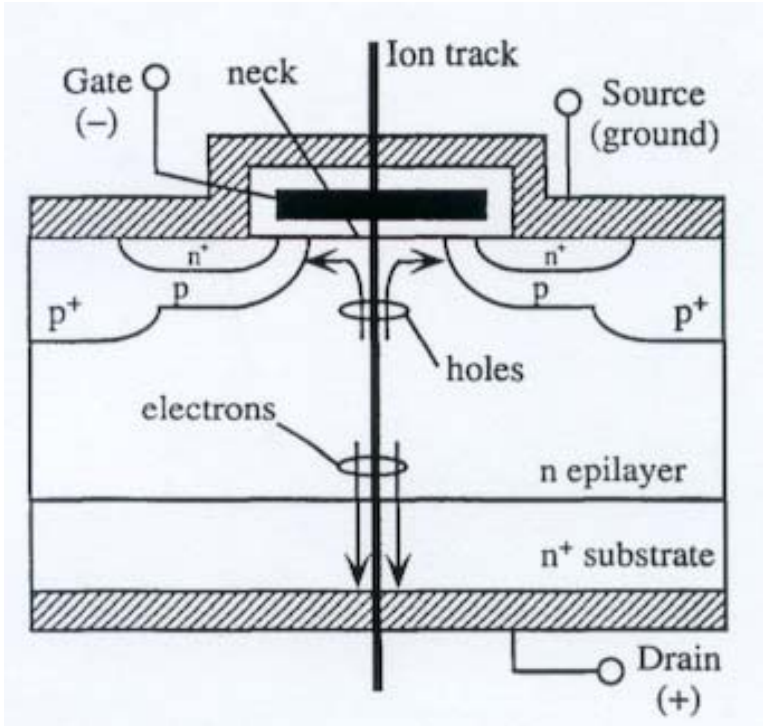
From previous curve and with analysis of the converter, it is possible to select a working condition where Vds of the MOSFET never exceeds 300V (this technique is called “derating” and is often used)



Safe area

SEGR in power MOSFETs

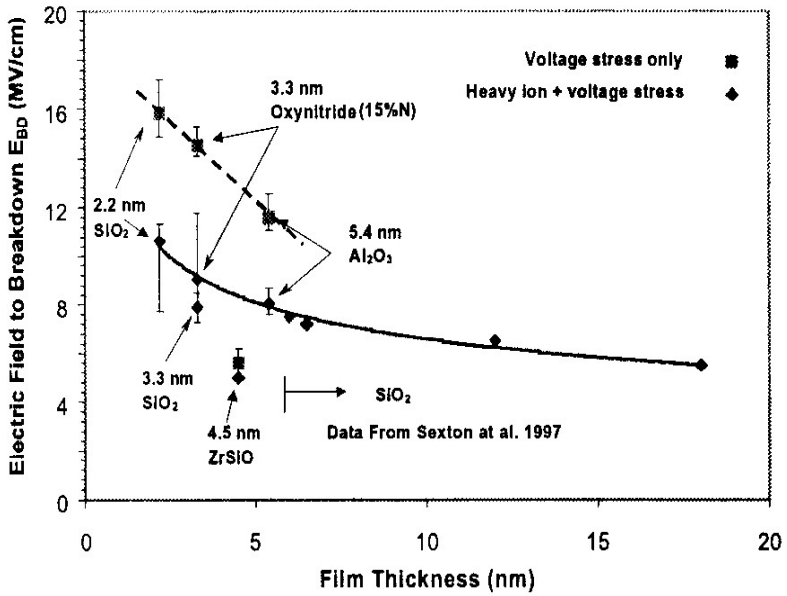
SEGR is caused by heavy-ion-induced localized dielectric breakdown of the gate oxide. SEGR test is destructive!

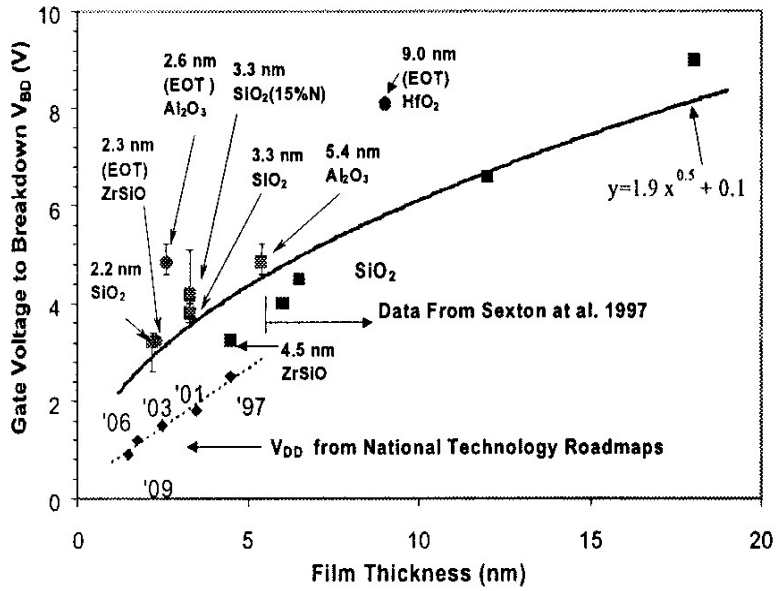


J.H.Johnson & K.F.Galloway, IEEE NSREC short course, 1996

SEGR in ULSI CMOS

Recent concerns in possible trend of SEGR in modern technologies





F.W. Massengill et al., "Heavy-Ion-Induced Breackdown in Ultra-Thin Gate Oxides and High-k Dielectrics", *IEEE Transactions on Nuclear Science*, vol. 48, no. 6, December 2001, pp. 1904-1912.

SEGR does not seem to be a problem even in the most advanced CMOS processes

Radiation effects in devices and technologies

Summary Table

Device	TID	Displacement	SEEs
Low voltage CMOS	Yes[1]	No	SEUs in logic and memories SETs relevant if fast logic (1GHz) SEL possible[2]
Low voltage Bipolar	Yes, with ELDR possible	Yes[3]	SEL extremely rare – if at all SETs
Low voltage BiCMOS	Yes	Yes	Combination of CMOS and Bipolar
Power MOSFETs	Yes	No	SEB SEGR
Power BJTs	Yes	Yes	SEB
Optocouplers	Yes	Yes	SETs
Optical receivers	Yes	Yes (tech dependent)	"SEUs"

[1]The threshold for sensitivity varies with technology generation and function. Typically failures are observed from a minimum of 1-3krd, and sensitivity decreases with technology node (130nm less sensitive than 250nm for instance)
[2]Sensitivity typically decreases with technology node. When Vdd goes below about 0.8-1V, then SEL should not appear any more
[3]Sensitivity depends on doping and thickness of the base, hence decreasing in modern fast processes

Particles and damages

Radiation	TID	Displacement (NIEL)	SEE
X-rays ^{60}Co γ	Expressed in SiO_2 Almost identical in Si or SiO_2	No	No
p	Equivalences in Si$^{\$}$ @60MeV 10^{11}p/cm^2=13.8krd @100MeV 10^{11}p/cm^2=9.4krd @150MeV 10^{11}p/cm^2=7.0krd @200MeV 10^{11}p/cm^2=5.8krd @250MeV 10^{11}p/cm^2=5.1krd @300MeV 10^{11}p/cm^2=4.6krd @23GeV 10^{11}p/cm^2=3.2krd	Equivalences in Si$^{\$,*}$ @53MeV 1 p/cm^2 = 1.25 n/cm^2 @98MeV 1 p/cm^2 = 0.92 n/cm^2 @154MeV 1 p/cm^2 = 0.74 n/cm^2 @197MeV 1 p/cm^2 = 0.66 n/cm^2 @244MeV 1 p/cm^2 = 0.63 n/cm^2 @294MeV 1 p/cm^2 = 0.61 n/cm^2 @23GeV 1 p/cm^2 = 0.50 n/cm^2	Only via nuclear interaction. Max LET of recoil in Silicon = 15MeVcm^{2}mg^{-1}
n	Negligible	Equivalences in Si$^{\$,*}$ @1MeV 1 n/cm^2 = 0.81 n/cm^2 @2MeV 1 n/cm^2 = 0.74 n/cm^2 @14MeV 1 n/cm^2 = 1.50 n/cm^2	As for protons, actually above 20MeV p and n can roughly be considered to have the same effect for SEEs
Heavy Ions	Negligible for practical purposes (example: 10^6 HI with LET=50MeVcm^{2}mg^{-1} deposit about 800 rd)	Negligible	Yes

$^{\$}$ Energy here is only kinetic (for total particle energy, add the rest energy mc^2)

*The equivalence is referred to “equivalent 1Mev neutrons”, where the NIEL of “1MeV neutrons” is DEFINED to be 95 MeVmb. This explains why for 1MeV neutrons the equivalence is different than 1

To study further…

- ✓ General material on radiation effects:
  - The best source is the “archive of Radiation Effects Short Course Notebooks, 1980-2006” collecting the courses given at the IEEE NSREC conference (CD sold by IEEE)
  - “Classic” books on the subject
    - “Ionizing radiation effects in MOS devices and circuits”, edited by T.Ma and P.Dressendorfer, published by Wiley (2001), ISBN 978-0471848936
    - “Handbook of radiation effects”, by A.Holmes-Siedle and L.Adams, published by Oxford University Press (2002), ISBN 978-0198507338
  - Recent Books with good overview of all effects:
    - “Radiation effects on Embedded Systems”, edited by R.Velazco, P.Fouillat, R.Reis, published by Springer (2007), ISBN 978-1-4020-5645-1
    - “Radiation effects and soft errors in integrated circuits and electronic devices”, edited by R.Schrimpf and D.Fleetwood, published by World Scientific (2004), ISBN 981-238-940-7
  - Best papers from the Nuclear and Space Radiation Effects Conference (NSREC) are published yearly in the IEEE TNS in the december special Issue
- ✓ Specialized conferences:
  - NSREC in the US, yearly in July
  - RADECs in Europe, conference (1 week) or workshop (2-3 days) every year in September