SEU effects in registers and in a Dual-Ported Static RAM designed in a 0.25 µm CMOS technology for applications in the LHC

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Abstract

A dedicated high-speed 18 Kbit static memory featuring synchronous mode, parity and dual port access has been designed and fabricated in a quarter micron 3 metals commercial CMOS technology. This SRAM has been designed to be a test vehicle to measure Single Event Upset (SEU) effects on a real circuit. The measurements have been performed at the cyclotron of Louvain-la-Neuve, Belgium, with a proton and heavy ion beam. We present the experimental cross-section curve for the RAM chip, together with a detailed study of the SEU phenomenon on dedicated test structures (shift registers) integrated in the same technology. Finally, we give an estimate for the upset rate the memory chip will experience in LHC.

1. INTRODUCTION

As a complementary solution to the use of dedicated radiation hardened technologies, we have recently proposed a design approach to increase the radiation tolerance of ASICs designed in commercial deep submicron processes [1]. Such approach, based on the use of enclosed geometry for the NMOS transistors and of guardrings, has lead to the design of circuits able to stand total doses in excess of 30 Mrad integrated in a quarter micron technology [2]. Since the use of guardrings also effectively protects the circuits from Single Event Latchup (SEL) [3], the main radiation-induced problem still needing to be investigated deeply is Single Event Upset (SEU). This is particular important since the trend points to an increased sensitivity to SEU with the down-scaling of CMOS technologies.

In this paper, we present results from heavy ion and proton irradiation of different test structures. From the measurements, we are able to estimate upset rates for basic building blocks in the LHC radiation environment. These results can be used by ASICs designers as a guideline on the architecture to choose for any given radiation environment in order to obtain an acceptable upset rate.

2. EXPERIMENTAL DETAILS

We have actually used two types of test structures in a commercial 0.25 µm CMOS process to validate our SEU measurements. In addition to a dual-ported static RAM, a set of shift registers has been implemented to evaluate the SEU sensitivity of basic building blocks used in ASICs design.

All the designs used the radiation tolerant layout practices described in [1] and aimed at hardening the circuits to total dose effects. Therefore, all NMOS transistors were designed with special geometries, and guardrings were extensively used across the circuit.

2.1 Memory array

The test structure most representative of a real circuit was an 18Kbit Synchronous Dual Ported Static RAM, organized in 2K x 9bit words (8 data bits plus 1 parity bit). This memory is a building block for a high-speed optical link interface ASIC being designed at CERN. However, it can also be used as a generic building block for read-out buffers or FIFOs.

The design features separate address and data busses for the Read and Write ports, thus allowing the execution of simultaneous Read and Write operations. Access operations to the memory are synchronous to the clock signal. A read cycle of the memory is shown in Figure 1, and a read access time of 13.3 ns was measured.

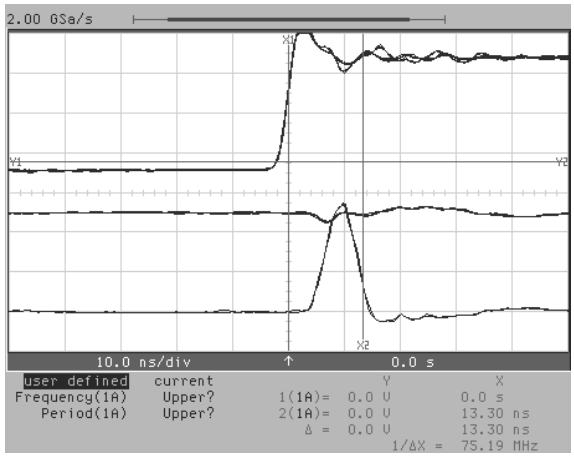

Figure 1: Snapshot of a sequence of read access cycles showing a read access time of about 13.3 ns.

The memory cell is based on conventional cross-coupled inverters design which has been expanded to a dual ported cell with the addition of two more pass transistors for a total of 8 transistors per cell.

The cell uses PMOS pass devices, as they are smaller than enclosed N type transistors. In addition, special care was applied in the design of the NMOS devices, to make them even smaller than what a conventional enclosed N device requires. The resulting size of the memory cell is only 5.90 µm x 9.94 µm. This is only about 5 times larger than the minimum single port RAM cell that one could achieve with this technology using the most aggressive design rules. The address decoding logic is built with a mixture of static and dynamic cells. Dynamic cells are used wherever it was estimated that SEU was not a potential danger, since some of the nodes – such as the write lines – have a very high capacitance associate anyway. These nodes are therefore relatively insensitive to SEU effects.

The layout of the memory is shown in Figure 2. The total area of the memory, including the read logic and the address decoders, is 1.18 mm^2. The memory chip has been fabricated in a 3 metal layer process. No substantial area improvement could be obtained with more metals, as the area is still dominated by the size of the devices in the cells and not by the routing resources.

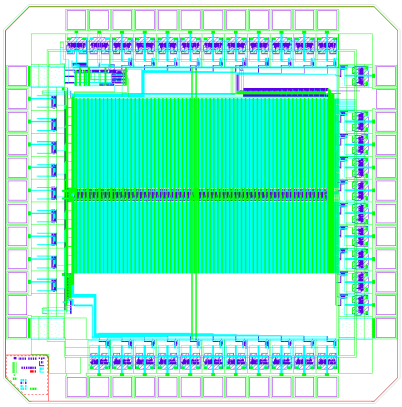

Figure 2: Layout view of the memory chip.

The layout of the memory has further been arranged to use a scrambled bit layout, i.e. adjacent bits in a word have not been placed adjacently in the layout, but they are placed far apart in the layout. This avoids that an ionising particle hitting between two adjacent bits could affect two bits in the same word.

The read logic in the memory array does not use sense amplifiers, which could speed up the access time if necessary.

2.2 Shift registers

To better study the SEU phenomena on clocked and unclocked circuits, and to be able to predict SEU rates in LHC for static and dynamic logic, we also integrated a series of shift registers made up of 1024 or 2048 identical flip-flop cells (DFF). The test of such devices is quite simple, and the interpretation of the results is simpler than for more elaborated circuits. Therefore, shift registers represent a convenient test vehicle to understand the SEU mechanisms and to validate procedures developed to estimate the SEU rate in the hadron-dominated LHC radiation environment.

Four different types of DFF, hence of shift registers, have been designed and irradiated to study the SEU. To compare the sensitivity of static and dynamic DFF architectures, we have designed two shift registers composed of, respectively, dynamic and standard static DFF cells. These cells were designed using the minimum transistor size compatible with the requirements of our radiation tolerant layout practice. Two modified versions of the static DFF cell were designed to decrease its sensitivity to SEU. In the first approach, some of the transistors have been designed with a bigger size to increase the node capacitance and the transistor current drive capability ("oversized" DFF cell). In the second approach, the capacitance of the sensitive nodes has been increased by adding a metal-to-metal capacitance on top of the cell ("overloaded" DFF cell). In both cases, the overall size of the DFF is unchanged with respect to the standard DFF.

2.3 Irradiation procedure

Single Event Upset measurements have been performed at the ESA-UCL line of the "Cyclone" cyclotron of Louvain-la-Neuve. Irradiation with both protons and heavy ions took place at room temperature, the particle flux being selected so that the probability to have double errors was always negligible. Figure 3 shows the measurement setup, composed of a mother board, a daughter board, and a laptop PC used as a terminal device.

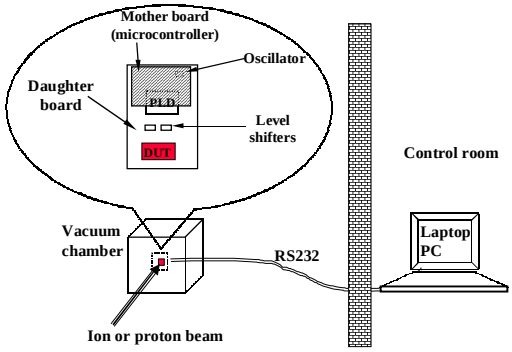

Figure 3: Measurement setup for the heavy ion irradiation. For the proton irradiation, the test board was not installed in a vacuum chamber, but in air.

On the daughter board, a Programmable Logic Device (PLD) is connected as and I/O peripheral to the microcontroller. The PLD provides all the necessary test signals to the Device Under Test (DUT) and, by monitoring its output signals, it also counts the number of SEUs. The daughter board can accommodate different types of test circuits by configuring appropriately the

PLD. Two different types of daughter boards were used in our tests, one for the memory and another for the shift registers. The test procedure run by the microcontroller was different for the two structures, as described below.

The test of the memory chips consisted of three phases. During the first phase, the entire memory space was filled up with a pre-selected data pattern. During the second phase no memory access operation was performed. This phase lasted for a predefined time period (1 s). During the third phase consecutive back-to-back read operations were performed and the memory contents were read out and compared with the data pattern originally written. The comparison gave the number of upsets encountered in the memory circuit. The operating frequency of the chip was 5 MHz.

The shift registers were tested in two modes of operation. In the "unclocked" mode, a pattern was pushed into the register at a frequency of 30 MHz, then the clock was frozen for a long time until another train of clock pulses was applied to shift the data out for error detection. In the "clocked" mode, the clock was constantly applied during the whole irradiation test at a frequency variable between 460 KHz and 30 MHz.

Protons accelerated at 60MeV in the main cyclotron were slowed down whenever necessary by inserting plastic moderators along the beam line. In this way, beams of energy down to about 10 MeV could be obtained. The flux used during the proton irradiation was about 10^8 p/(cm^{2}s), and the circuits were exposed always at normal incidence.

For the heavy ion test, the effective Linear Energy Transfer (LET) of the ions could be varied between 6.1 and 74 MeVcm^2/mg. This was possible either changing the ion species (Neon, Argon and Krypton were used) or by tilting the circuit of an angle with respect to the incident beam (up to 60^o). In the heavy ion case, the flux was varied between $5 \cdot 10^3$ and 10^4 particles/(cm^{2}s).

For each test, with protons or heavy ions, the errors were counted until the desired particle fluence was reached. The ratio of the errors over the fluence, normalized to the number N of memory points (or DFF cells) in the circuit, gives the cross-section value for the given proton energy of heavy ion LET:

σ = Errors/(Fluence·N)

Repeating the test for different proton energy and for different LET, we could trace the complete cross-section curve that fully characterizes the SEU sensitivity of the circuits under test. The measured points in such a curve are normally fitted using a Weibull function [4]:

$$\sigma = \sigma_{sat}\left\{1 - \exp\left[-\left(\frac{LET - LET_{th}}{W}\right)^S\right]\right\}$$

where σ_{sat} is the saturation cross-section, that is the total area of the circuit sensitive to SEU, LET_{th} is the threshold under which the circuit is not sensitive to upsets, W and S are two shape factors.

3. RESULTS AND DISCUSSION

In this chapter, all cross-sections referring to the heavy ion irradiation test are plotted as a function of the effective LET. Such effective LET is calculated in the hypothesis of an 8 µm thick layer of silicon dioxide above the sensitive region. The sensitive region of the circuit is in the silicon itself, and is covered by several layers of silicon dioxide (planarization for metal layers and surface passivation).

3.1 Memory

The memory circuit was irradiated while powered at V_{dd}=2.5 V with heavy ions up to an effective LET of about 32 MeVcm^{2}mg^{-1}. Even though at the maximum LET used in our test the saturation cross-section was not yet reached, the explored LET region is the most significant for our aims. In fact, to predict the upset rate for a circuit in LHC, we need to have good Weibull fit parameters in the LET region representative of the fragments produced by nuclear interaction of hadrons in silicon. The LET of such fragments do not exceed 15 MeVcm^{2}mg^{-1}.

The cross-section curve measured for the memory chip is shown in Figure 4, where the solid line represents the Weibull curve fitting the experimental points. This curve was drawn writing a pattern of alternate 1's and 0's in the memory, but very comparable results were obtained with "all 0" and "all 1" patterns, proving that there is no enhanced sensitivity for either high or low values stored in the memory. This is obvious and expected, as the memory cell actually stores both 0's and 1's anyway.

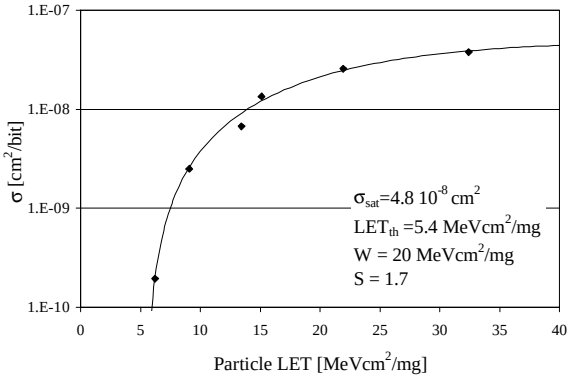

Figure 4: Cross-section curve for the memory circuit irradiated with heavy ions. The measured points are fitted with a Weibull function (solid line), and the fitting parameters are reported.

With the Weibull parameters, and using the method described in [5], we can estimate the upset rate this memory chip would experience in different points of the

CMS experiment. The method is based on an extensive simulation work, and we will use it with the hypothesis of a cubic Sensitive Volume (SV) of 1x1x1 μm^3. The results of such calculation are reported in Table 1 for different positions in CMS: in the pixel detector (η=0-0.9, R=0-20 cm), in the outer tracker (η=0-0.9, R=65-120 cm), in ECAL behind the endcap (R=50-130 cm), in the experimental cavern above the endcap (R=700-1200 cm).

Table 1: Estimate of the upset rate for the memory chip in several positions of the CMS experiment at peak luminosity. The estimated cross-section Σ multiplied for the particle fluence Φ gives the upset rate Φ x Σ (upset/chip·s).

	> 20 MeV hadr.		2-20 MeV neutr.	
Region	Σ (cm^2)	Φ x Σ	Σ (cm^2)	Φ x Σ
Pixel	$3.4 \cdot 10^{-11}$	$2.0 \cdot 10^{-4}$	$2.2 \cdot 10^{-13}$	$1.2 \cdot 10^{-7}$
Outer tracker	$2.1 \cdot 10^{-11}$	$2.1 \cdot 10^{-6}$	$2.3 \cdot 10^{-13}$	$1.7 \cdot 10^{-8}$
Behind Endcap	$2.2 \cdot 10^{-11}$	$6.6 \cdot 10^{-6}$	$1.2 \cdot 10^{-13}$	$1.7 \cdot 10^{-8}$
Exp. Cavern	$1.4 \cdot 10^{-11}$	$1.2 \cdot 10^{-9}$	$8.2 \cdot 10^{-14}$	$7.6 \cdot 10^{-12}$

From Table 1, one can see that the upset rate is always dominated by hadrons (including neutrons) of energy above 20 MeV. The contribution from thermal neutrons has been neglected, as it has been shown to be well below that of high-energy particles [5]. The possible exception is for devices with very high boron doping, but the estimate in that case would require the knowledge of the precise doping profile of the chip, which is most often unknown to the designer.

The highest total (> 20 MeV hadrons + 2-20 MeV neutrons) upset rate of $2 \cdot 10^{-4}$ is found in the pixel detector. If we assume that LHC will run for $5 \cdot 10^7$ seconds in the foreseen 10 years of its operation, the memory chip will experience a total of about 10000 upsets. In the outer tracker the estimated total number of upsets falls to about 105, behind the endcap of ECAL it is 330, and no upset are expected for this memory in the experimental cavern.

3.2 Shift registers

The shift register circuits have been irradiated with heavy ions and protons in both the "unclocked" and the "clocked" operation mode.

The cross-section curves measured with a heavy ion beam are shown in Figure 5 for the dynamic shift register (clocked mode) and for the standard static shift register (clocked and unclocked mode). The experimental points are fitted with a Weibull curve in the three cases, but the confidence level of the fit is not extremely high since the number of points is very limited. This is especially true in the LET region close to threshold, where the sensitivity of the cell decreases.

Two important tendencies can be noticed in Figure 5. The most striking is the much higher sensitivity of the dynamic shift register if compared with the static one. Additionally, the static shift register is more robust to SEU when it operates in the unclocked mode.

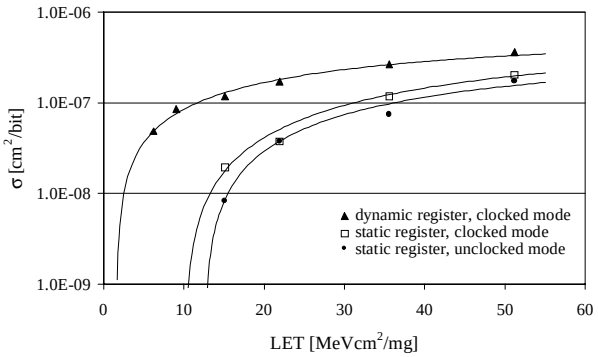

Figure 5: Measured cross-section for dynamic and static shift registers with a heavy ion beam. Experimental data are fitted with a Weibull curve in all cases. The frequency of the clocked test was 30 MHz.

With the above explained limitation on the confidence level of the Weibull fit, we can use the fitting parameters to estimate the upset rate these shift registers would experience in LHC, as already done for the memory. Also in this case, we will make the hypothesis of a cubic SV of 1x1x1 μm^3.

To have a more significant estimate for real ICs integrating a large number of DFF cells, we will make the calculation for a number of 10^6 cells. The results for the three cases are reported in Table 2. In the clocked mode, the rates for the dynamic DFF are more than two orders of magnitude larger than for the static DFF.

Table 2: Estimate for the upset rate for 10^6 DFF cells in different positions of the CMS experiment. The estimate is for the total upset rate, including the effects of all charged hadrons above 20 MeV and neutrons above 2 MeV.

	Upset rate [errors/(10^6 cells · s)]		
Region	Dynamic DFF	Static DFF "clocked"	Static DFF "unclocked"
Pixel	$7.1 \cdot 10^{-1}$	$3.2 \cdot 10^{-3}$	$3.0 \cdot 10^{-4}$
Outer tracker	$9.7 \cdot 10^{-3}$	$2.5 \cdot 10^{-5}$	$1.8 \cdot 10^{-6}$
Behind Endcap	$3.1 \cdot 10^{-2}$	$9.5 \cdot 10^{-5}$	$1.1 \cdot 10^{-5}$
Exp. Cavern	$7.3 \cdot 10^{-6}$	$1.5 \cdot 10^{-8}$	$2.1 \cdot 10^{-9}$

To verify whether the two modified versions of the static DFF cell, the "oversized" and the "overloaded" cells, have an improved SEU cross-section over the standard cell, we have irradiated them with heavy ions. The resulting cross-sections are reported in Figure 6, where they are compared with the behaviour of a standard static cell integrated in the same test chip. This figure refers to the clocked mode, at a frequency of 30 MHz.

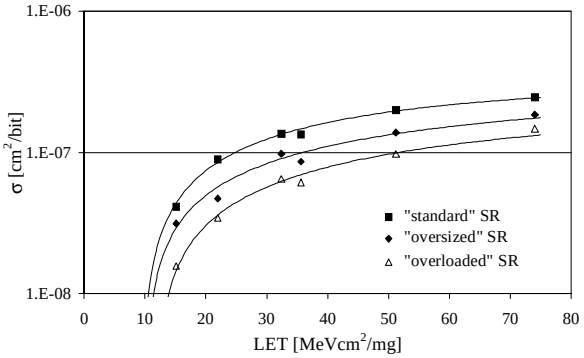

Figure 6: Measured cross-section for the different static DFFs irradiated with heavy ions in the clocked mode.

The modified cells are less sensitive to SEU than the standard DFF, with the "overloaded" solution being the most effective. This cell pays a penalty in terms of speed and power consumption, but it still easily complies with most of the applications in ASICs for LHC, where a speed of 40 MHz is a standard requirement. The use of the Weibull fit parameters to estimate the upset rate for these cells in LHC reveals that the upset rate for the "oversized" DFF is almost a factor of 2 lower than for the standard DFF, this factor increasing to 10 for the "overloaded" cell.

To understand how precise are all the above estimates for the LHC environment, we can use the same method to estimate the upset rate for a proton beam irradiation. This estimate can then be compared to the experimental results. We have irradiated the dynamic and the standard static shift registers with a proton beam, and varied the energy of the incoming protons between 10 and 60 MeV. The measured cross-section curve as a function of the proton energy is shown in Figure 7 for the dynamic register clocked at a frequency of 30 MHz. The cross-section gets lower when the power supply voltage is decreased to 2 V, in contrast with the common idea that the SEU sensitivity is higher at lower V_{dd}.

If we compare the experimental cross section at 2.5 V with the estimate obtained from the Weibull parameters of the fits in Figure 5, we observe that the estimate is a factor of about 4 lower when we assume a cubic SV of 1x1x1 μm^3. When the SV thickness is decreased to 0.5 µm, the under-estimate reduces to a factor of 2 only, which is quite a satisfying result also when considering the already discussed poor quality of the fit in Figure 5. It appears that the 1x1x0.5 μm^3 is a better guess for the sensitive volume in this technology, and that the assumption of that SV size leads to more reliable estimates. Nevertheless, the necessary simulations for such SV size are not at present available, and all the estimates for the LHC environment presented in this work have been done for a cubic SV. According to the comparison for the dynamic DFF, such estimates might actually under-estimate the real rate. This should be considered when using these results.

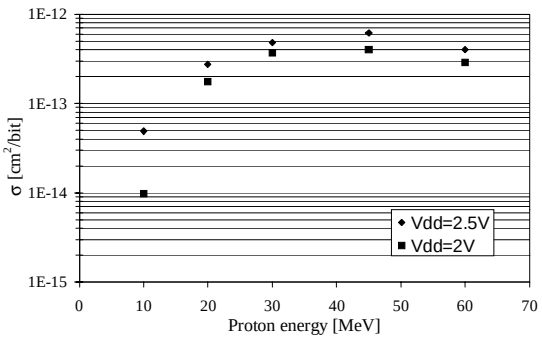

Figure 7: Measured cross-section for the dynamic shift register irradiated with a proton beam at different power supply voltages in the clocked mode.

4. CONCLUSION

SEU cross-sections have been measured for a 18Kbit dual-ported static RAM and for a set of test shift registers. From the Weibull curves fitting the experimental points, the upset rates for such circuits in the LHC radiation environment have been estimated.

The heavy ion irradiation of the memory has revealed a LET_{th} of about 5.4 $MeVcm^2/mg$, higher than for most state-of-the-art commercial SRAMs [6]. We have estimated for such chip an upset rate in LHC varying between $2 \cdot 10^{-4}$ and $1.2 \cdot 10^{-9}$ errors/s, respectively in the pixel detector and in the experimental cavern.

Measurements with both heavy ions and protons have confirmed that dynamic DFF architectures are at least two orders of magnitude more sensitive to SEU than static ones in the LHC environment. Simple approaches with no area overhead are effective in decreasing the sensitivity of the static DFF cell. In particular, the implementation of an additional metal-to-metal capacitance to load the sensitive nodes has lead to a tenfold decrease in the SEU sensitivity.

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